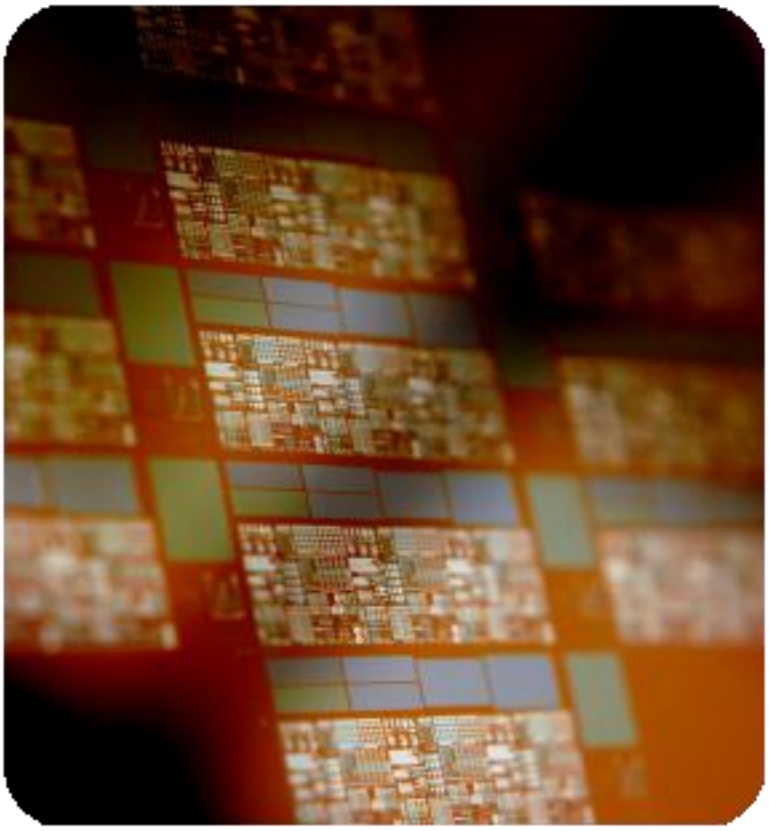
ECE444

Theory and Fabrication of Integrated Circuits Laboratory



Operating Procedures

Summer '18

Table of Contents

Appendix A

ICS – Interactive Characterization Software

ICS is an instrument control and data acquisition program used to characterize electronic devices.

To minimize the learning curve of the test instruments, ICS uses a simple graphical interface to setup the instruments for electrical testing. All that is required to create a test setup is the selection of the instruments used, the type of device, the placement of test leads on the device schematic, the voltage(s) or current(s) delivered to the terminals, and the electrical parameters to be measured.

The overwhelming majority of ECE444 students are ECE majors, so testing will not be laid out in as much detail as the chemistry type procedures which are used to create the devices.

We have prepared some basic, safe models and setups for you to use, but in almost every case, there are modifications which can, and therefore should, be made to the setups in order to exhibit as much useful information about your particular device as possible

The object will be to apply your knowledge of the devices to make these adjustments. For example, don't settle for plots in which all the "action" happens along one edge

.In addition, some setups will function as given to the student; however, the setup will return meaningless data – the lab requires you to think! Dig out the ece440 text.

Starting ICS

ICS is installed on the PCs in the laboratory. To start, double click the icon on the desktop labeled ICS. If the desktop link does not work or if there is no icon, click on **Start →Run**, then type **ics** and press **OK**.

File Structure

ICS stores data and setups in a database file located in your ***W:\data folder*** (the ***W:*** drive should be automatically mapped when you log into the PC workstation).

You will need to manually copy a 'template' folder to your W: drive.

- Navigate to the ***V:\ece444*** folder (it should be automatically mapped; if not, let your TA know)
- Copy the ***ICS_Files*** folder
- Paste the ***ICS_Files*** folder in your ***W:*** drive

This folder initially contains all of the test setups for testing both the commercial devices and your wafer. The data file for the prelab is also included.

The test setup files copied above must be mapped in ICS to use them.

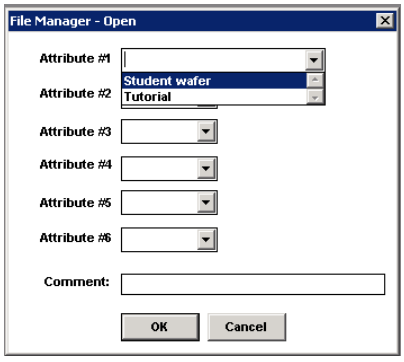
- Click on ***File→File Manager Setup…***
- The File Manager Setup window will appear. Click ***Cancel***.
- Click on ***File→File Manager Setup…*** (again)
- The **File Manager Setup** window will appear – this time the **Database Directory** text box will be populated with all mapped drives.
- Scroll down until **[-w-]** appears. Double click on **[-w-].** Double click on **[ICS_Files]**. Double click on **[data].**
- Click ***OK***.

This procedure may need to be repeated when switching to a different workstation.

ICS now knows where the data files are located, and will save to this location.

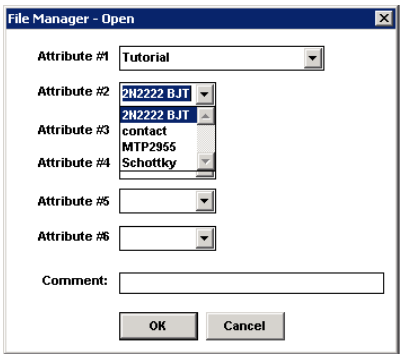
Opening a File

To view the test setups, start ICS and select ***File→Open…*** A window named **File Manager – Open** will open with six **Attribute** pull down boxes. The choices for **Attribute #1** will be:



Select **Tutorial** for **Attribute #1.**

Once **Attribute #1** is selected, **Attribute #2** will display the available test setups. The choices for **Attribute #2** will be (with **Tutorial** selected):



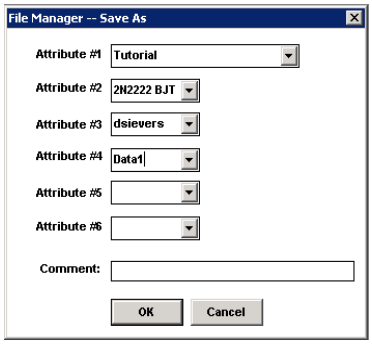
Select **2N2222 BJT** for **Attribute #2** and click ***OK***.

The **File Manager** will close, and the test setups for the BJT will open in the main window (they will be minimized).

Saving Data

At this point save the **2N2222 BJT** setup by selecting **File→Save As…**

The **File Manager -- Save As** window will open, allowing additional attributes to be entered for organization.



Add the following Attributes:

- Attribute #3: *netID*
- Attribute #4: *Data1*

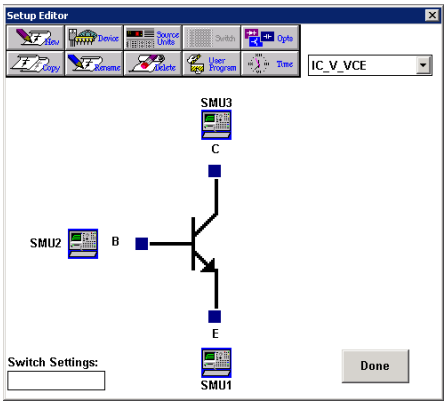
Click ***OK*** to save the data with your personalized attributes.

Note: Attribute #4 allows you to separate different sets of similar data. If three different 2N2222 devices are tested, they would use the same test setup, but would be saved using different Attribute #4 identifiers (e.g. Data2, Data3, etc.).

Test Setup

To view the parameters for the tests after loading them onto the main window, click on the **Edit Test Setup** button at the top of the window.

The **Setup Editor** window will appear with a schematic of the device being tested and the leads from the measuring instrument connected.



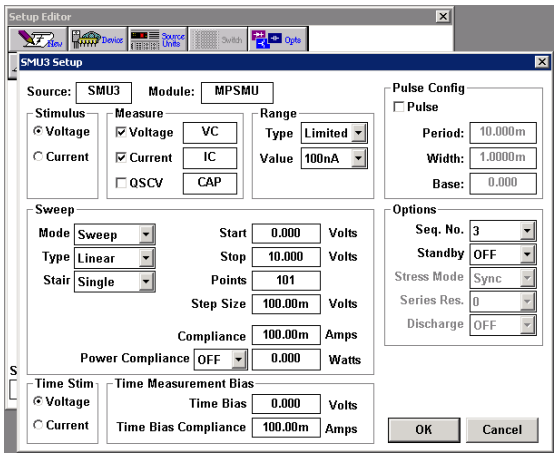
In the upper right-hand corner is a drop-down list of the test setups (in this example, **IC_V_VCE**). You can change the test setup by selecting a new test from the drop-down list.

The main area of the editor contains a schematic diagram of the device being tested (in this case, an npn BJT) with each of the leads labeled (**E=emitter**, **B=base**, **C=collector**) and the test leads from the instrument connected to each lead of the device (**SMU1** to **E**, **SMU2** to **B**, **SMU3** to **C**).

To view and modify the test conditions, double click the instrument lead box connected to the device. For this example, click **SMU3**. The **SMU Setup** window will open with the current test conditions for the lead displayed.

The options available for the lead are dependent upon the test instrument connected. This lead (**SMU3**), connected to an Agilent 4155C, will:

- act as a voltage source
- measure and return Vc, Ic values
- perform a single linear sweep
- 0 – 10 volts
- 100mV resolution
- 100mA compliance



The test instrument connected dictates the options available – your TA can explain the available configurations. To close the window, click ***Cancel*** (don't change what has been setup already).

Testing

Next, let's look at the test displays in the main window. There are two types of windows for the tests – data windows and graph windows. You can tell the two apart by their icons:

Open the minimized **IC_V_VCE** data window by double-clicking the *title bar* or single clicking the ***Restore*** or ***Maximize*** buttons. You will see an empty spreadsheet. Once a device is tested the returned data is stored here (temporarily unless saved).

Open the **IC_V_VCE** graph window. You will see a black screen with **ICS||||** in the middle. Since nothing has been tested, there is no data to display.

In order to populate the test setup, the test must be run. Click on the ***Measure*** icon at the top of the main window.

This will open the **Measure** window. At the top is a drop down box with available tests for the device.

The active spreadsheet or plot window will determine the initial test selected. To select another test setup, select it from the drop down box. To initiate a test, press ***Single***.

If you wish to stop the test for any reason, press ***Stop***.

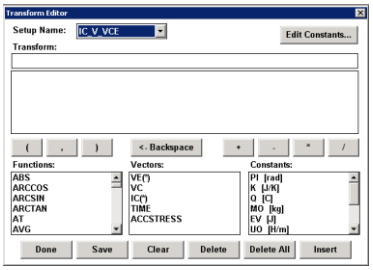
After pressing ***Single***, the commands for executing the test are sent to the instrument. The instrument performs the test and sends the results back to ICS. If there are any problems encountered, a message box will popup describing the problem (press OK to close the message).

The returned data is then placed in the spreadsheet and any data tied to a graph is then displayed.

Transforms

Not all data can be directly measured. An example would be transconductance of MOSFET devices $\left[\frac{d}{}\right]$.

To create a transform, click on the **Transform Editor** button.



The **Transform Editor** window will open with the active setup as the default setup.

To add a transform, type in a name for the transform in the box labeled **Transform:** and set it equal to the mathematical expression desired. For example:

$$gm = DIFF(ID,VG)$$

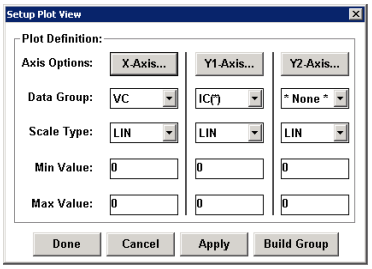
The available functions are listed in the function box. You can add the variables measured by selecting the appropriate variable name under **Vectors**. Common constants are also listed.

Once created, click **Save**. The transform is then listed in the larger box. When you are done adding transforms click on **Done**.

Modifying Plots

The data gathered by ICS can be plotted. Click on the **Setup Plot View** button at the top of the main window.

The **Setup Plot View** window will appear with the setup information for the currently active plot window.

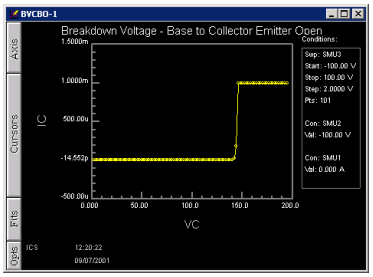


You can add or modify the plot axes by selecting the appropriate variable name under **Data Group**. All data that was selected to be measured in test setup is available for plotting, as well as any transform created for the setup. You can also specify scale type (linear, log, etc.) and minimum and maximum values of the scale.

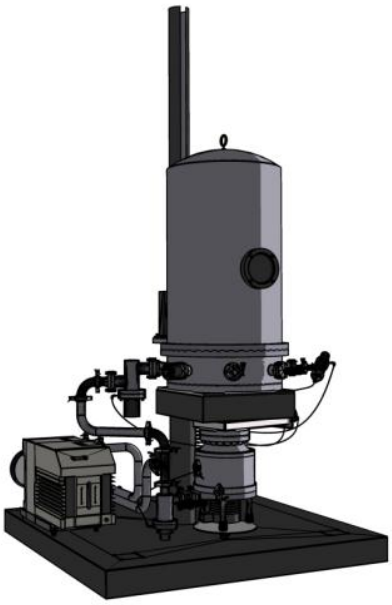
Adjusting Plots

The **Plot Window** has a menu bar along the left side. To access the features click on the appropriate menu item.

Axes can be auto scaled, cursors added, and linear line fits can be performed. There are also options for the appearance of the plot, zooming, and overlaying multiple plots.



Appendix B



Thermal Evaporation

The 7211 was custom-built specifically for the eceE444 lab by Dane Sievers and Leon Schneider. It has the capacity to evaporate aluminum onto nine 4" wafers. The evaporation of metal is performed under high vacuum, with consistent, high quality films.

Thin film deposition can be performed using many different methods. The 7211 uses one of the simplest: evaporation.

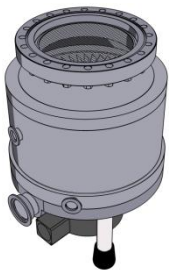
To evaporate metals thermally, a wafer is placed inside an air-tight chamber. Vacuum pumps reduce the pressure inside the chamber. Once the atmosphere is sufficiently reduced for a clean deposition, aluminum is heated using a resistively filament. As the temperature rises to the boiling point of the metal, it begins to evaporate. The evaporated metal will then condense on all surfaces in the chamber, including the wafer.

In order to evaporate pure films, the process must be performed under ultra-high vacuum (UHV). The ideal pressure is ~10^{-7} Torr, which will result in a mean free path of ~100 m – this is the average distance a particle will travel before it hits another particle (walls don't count). Achieving this vacuum level requires careful preparation, absolute cleanliness, specialized vacuum pumps, and appropriate instrumentation to measure pressure.

Vacuum Pumps

Many parts for the LDS 7211 were chosen based on their availability, provided they would not compromise the robustness and functionality of the overall system. The following sections describe the parts used in the ece444 Lab's evaporator.

Turbomolecular pump
Leybold TMP1000C



The high-vacuum pump used in the system is a turbomolecular pump featuring grease-lubricated bearings. Turbomolecular (or 'turbo') pumps work on the basis of momentum transfer to gas molecules or atoms (we'll call them particles).

Turbo pumps have a series of precisely balanced rotors spinning at very high rotational velocity (36,000 rpm) along the main axis of the pump. The pump is usually connected directly to the vacuum chamber; a high-vacuum valve allows the pump to be isolated from the chamber for venting to atmospheric pressure.

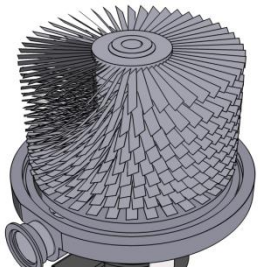


Figure 1: exposed rotors

The gas to be pumped out of the chamber arrives at the inlet by random motion (the pressures the pump operates within are in the free molecular range). When the particles impact the spinning rotors, momentum is transferred from the rotor to the particle with a downward velocity component.

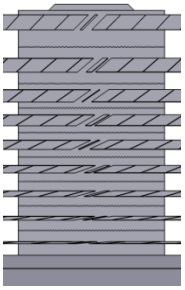


Figure 2: rotor pitch

The rotors at the top of the pump have a higher pitch than those at the bottom. Thus, each stage becomes more 'opaque' than the previous, minimizing the chances of a particle re-entering the chamber.

As the particles are pushed to the bottom of the pump, they are compressed to a pressure suitably high enough for a rotary vane pump to efficiently remove.

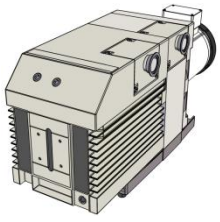
It is critical that the compressed gases be removed to maintain a pressure that is low enough to reduce frictional drag on the lower stage rotors. If the pressure is too high in the exhaust of the pump, the rotors will be slowed down; the pump controller is designed to maintain a constant velocity and will increase the drive current to the motor that spins the rotors. This current can be increased to a level that will overheat the motor or destroy the drive transistors.

Turbo pumps work from a range of ~10^{-2} Torr down to less than 10^{-10} Torr. At pressures above 10^{-2}, the molecular flow of gases turns into a laminar viscous flow, which causes excessive loading of the motor due to frictional drag. A pressure of ~10^{-2} must be maintained on the foreline (exhaust) side of the pump to ensure extreme pressure differences do not cause the pump to fail.

With the proper procedures followed, the pump is very reliable and requires little to no maintenance.

The TMP1000C operates at 36,000 rpm when at full speed, with acceleration, deceleration, and operational speed controlled by a Leybold Turbotronik NT1000 frequency converter. The NT1000 is extremely simple to operate, with only 'Start' and 'Stop' buttons, and provides feedback to the user about current pump status.

Roughing Pump



The roughing pump, a Leybold D65BCS, provides two functions in the 7211. First, it pumps the vacuum chamber from atmospheric pressure down to low vacuum (~10-2 Torr). Second, it maintains vacuum on the foreline side of the turbo pump, ensuring that the turbo will function properly.

The D65 is an oil-sealed two-stage rotary vane pump. This type of pump consists of two cylinders, each of which has a rotor, offset from the center line and tangent to the edge of the cylinder. Slots in the rotor hold sliding vanes that follow the outer chamber as it rotates. These two points of contact with the cylinder form the boundaries of a variable volume. The side of the cylinder in which the vanes form an increasing

volume is the intake – remember pV=nRT; as the volume increases, the pressure decreases and draws gas into the intake volume. As the rotor continues to turn, this volume begins to decrease – once again the ideal gas law holds and the pressure increases, forcing the gas out the exhaust. The cylinder is lubricated with oil, which also creates a tight seal with the rotor and vanes

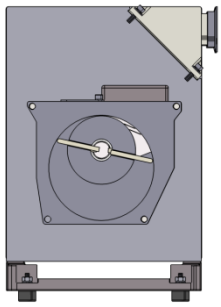


Figure 3: cross-sectional view of rotary vane pump showing vanes.

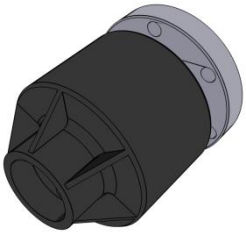
The oil seal limits the rotary vane pump to mTorr pressures (typically 0.1 – 1 mTorr). During operation, gas from the exhaust side (compression) will 'bubble' through the oil film – a 'leak'. At high inlet pressures, this 'leak' is insignificant. As the inlet pressure decreases, the 'leak' will ultimately equal the amount of gas that enters the inlet from the system, effectively preventing the pump from lowering the pressure any further on the inlet side – the leak rate is equal to the pumping speed at the pump's ultimate pressure.

A two-stage rotary vane pump can achieve a lower pressure than a single-stage pump due to a smaller pressure delta between the inlet and exhaust of the first stage.

Pressure Transducers

The 7211 uses a total of three pressure transducers. Two of these are connected directly to the vacuum chamber and measure low vacuum and high vacuum separately, and the third is connected to the foreline side of the turbo pump. Two different types of transducers are used: *cold-cathode gauges* and *Convectron gauges*.

Cold Cathode Gauge



The high-vacuum gauge connected to the chamber is a HPS Type 423 I-Mag inverted magnetron cold-cathode gauge. Cold-cathode gauges are electrical gauges, meaning that they measure pressure indirectly, in terms of the number density of molecules. Cold-cathode gauges fall under a specific category of electrical gauges, called ionization or *Penning* gauges, which use electron impact to produce a measurable ion current.

Cold-cathode gauges contain two unheated electrodes between which a DC discharge will occur at sufficiently high electric fields. The discharge is maintained via ionizing collisions between e^-s and gas particles, and is assisted by the use an external magnetic field (which causes the charged particles to spiral and travel a longer distance before neutralization, following the relationship $r = \frac{1}{B}\sqrt{\frac{mV}{Zq}}$). An ion current can be measured between the two electrodes, and the magnitude of this current indirectly indicates a measure of pressure – as the pressure decreases, there are fewer ionizing collisions and the ion current decreases.

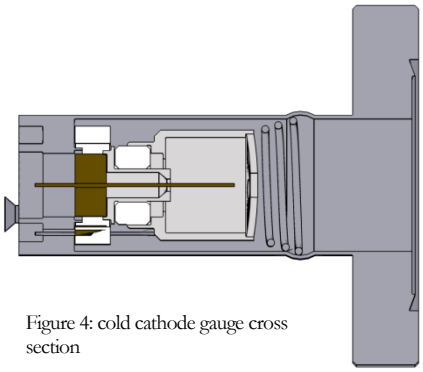


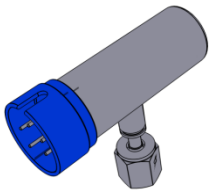
Figure 4: cold cathode gauge cross section

Cold cathode gauges can measure pressures as low as ~10^{-10} Torr; pressures below this value have little effect on the electrical discharge, and the ion current remains constant. Above the ~10^{-2} Torr limit, the cold cathode gauge should be powered down through its control system to prevent damage due to large ion currents (higher gas density increases ion current).

The HPS Type 423 gauge used in the 7211 measures pressure as low as 10^{-10} Torr, is compact, and relatively inexpensive. There is no internal heated filament as in a traditional ion gauge, making the cold cathode gauge more resistant to vibration, debris, and sudden inrushes of air.

Convectron Gauges

The other two gauges in the 7211, the low-vacuum chamber gauge and the foreline gauge, are Convectron gauges. These are enhanced Pirani gauges which provide rapid response, a wide range of pressure transduction, stable operation, and good accuracy.



The main sensor, which forms one branch of a Wheatstone bridge, is a very fine heated wire. The wire cools down as gas molecules collide with it; thus it will lose more heat as the gas pressure surrounding it increases. The heat lost from the sensor is determined by measuring the heating power that is delivered to it, while the Wheatstone bridge provides feedback for the constant temperature controller supplying current to the filament.

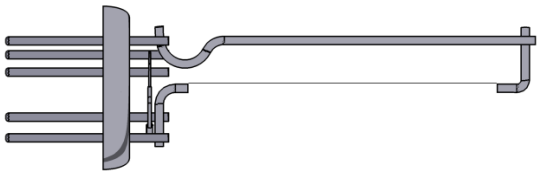


Figure 5: convectron gauge showing exposed filament

Figure 6: convectron gauge showing compensator wire

The Convectron is similar to a Pirani gauge but adds convection cooling to extend the measurement range up to 1000 Torr. A relatively large volume inside the gauge allows convection currents to develop. A larger wire wrapped around a cylinder enclosing the sensor, called a compensator, adjusts the operation of the gauge so that it performs relatively independent of the ambient temperature. The gauges on the system measure from 1000 Torr down to approximately ~10 Torr.

Gauge Controllers

To control the pressure transducers and provide feedback to the user, the LDS 7211 uses an MKS146A Vacuum Gauge Measurement and Control System. The 146A can monitor up to four vacuum gauges of varying types and provides readings from atmospheric pressure down to ~10^{-10} Torr.

For each gauge, the 146 can display the current measured pressure or the leakage rate at that gauge. Additionally, the 146 can be used to control valves, trigger alarms, and provide computer control via RS-232.

Miscellaneous Equipment

The remainder of the equipment comprising the system controls the evaporation of metal: in-situ thickness measurement, filament power supply, chamber, chassis, and valve control switches.

IC6000

The IC6000 deposition controller provides both accurate film measurement and total deposition control. Six different film programs can be entered, each with 37 different specifiable operating parameters.

A data display gives the deposition rate, thickness, power, process time, crystal condition information, and a histogram of deposition rate.

When the aluminum deposition is actually performed, the deposition controller, in conjunction with a Concordia power supply, is used to control and monitor the process. The IC6000 and power supply can be used as totally automated instruments, completing the entire deposition process automatically through predefined recipes.

The IC6000 allows for different film types (gold, aluminum, etc.), different rates, and a variety of features. In its current use, the IC6000 simply monitors the deposition rate and total amount for a given film type. Monitoring is done with a Leybold crystal sensor located at the same level as the wafers.

Concordia AC Power Supply

The Concordia ac power supply is used to supply the high current necessary to melt and evaporate the aluminum pellets. The current is adjusted with a rotary knob on the unit and displayed on a digital readout.

The power supply can output 0-120V. The output is connected to a 10:1 step down transformer. The output of the transformer is then connected to a tungsten filament (boat), which acts as a heater to melt the aluminum through $I2^R$ heating.

Chamber and Chassis

The support system, planetary, and other mechanical components were all designed or modified specifically for use on the 7211. The frame of the system was designed to allow for balance and stability of the entire system, while allowing students to quickly gain an understanding of the entire process flow. Additionally, the current design makes system upkeep and repair relatively easy for a system this size.

The hoist system for the bell jar, part of a Varian 3120 evaporator, was modified to support the new jar and provide a counterweight system for safety.

Inside the vacuum chamber, two parallel copper bars connected to the output of the step-down transformers, provide an easy way to add aluminum pellets to the system and replace the boats in case of breakage.

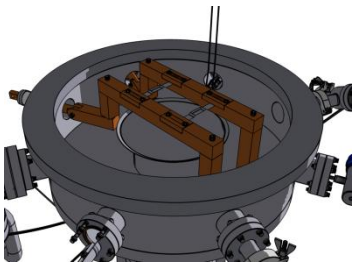


Figure 8: copper bus bars for filament

The wafer holder, which holds nine 4" wafers simultaneously, is well above the aluminum pellets, increasing the uniformity of the film thickness deposited. It is freestanding, making future upgrades to larger and different wafer sizes easy.

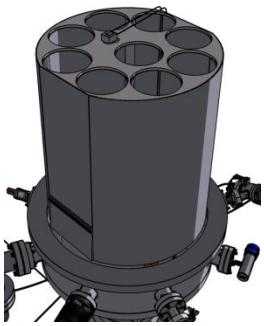


Figure 7: shroud with wafer holders

The valve system, with the exception of the manual needle valve for the turbo pump, is done pneumatically. Each valve is controlled by a solenoid, which is in turn controlled by a series of relays and switches in the equipment panel.

The relay system allows for interlocks to be integrated, ensuring correct system operation. A ladder diagram of the relay system is included in the attached list of figures.

Automated/Manual Switching

The LDS evaporator can be controlled either from the manual switch panel or from the PC using the touch-screen display.

The system operating mode (manual/automatic) is controlled by a keyed switch. Only the lab engineer should switch states, as valve state must match between the switch panel and PC display or damage to the system may result.

Manual Mode: When in manual mode, all operations are performed via the control rack. This mode is considered 'expert' mode and should only be used if there is a problem with PC control.

Supervision by the lab engineer is required when running in Manual Mode.

Automatic PC Mode: Normal operation is performed using the touch-screen interface. To operate, the user accesses functions by touching the appropriate button on the display.

This mode is a 'safe' mode, providing full interlock functionality to prevent incorrect valve states, thus preserving the integrity of the equipment.

Operating Procedures

Standby State

When not in operation, the chamber must be held at high vacuum to maintain cleanliness and minimize pump-down times.

Standby Configuration	
Hi-vac valve	ON
Foreline valve	ON
Roughing valve	OFF
Vent valve	OFF
CCG	ON
IC6000	OFF
Power supply	OFF
Rouging pump	ON
Turbo pump	ON

Opening the Chamber from Standby

1. Close the high-vac valve. The system will not allow any valve to change state until the valve is fully closed.
2. Turn off the cold cathode gauge by pressing 'CCG' on the monitor.
3. Open the vent valve.
4. Once the chamber is at atmospheric pressure (~760 Torr), raise the bell jar using the switch on the rack-mounted control panel.

Loading

1. Carefully load 4" wafers face down in platen and place the wafer cover over the wafer.
2. If less than nine wafers are being processed, fill the remaining holes with the wafer covers.
3. Double-check to make sure the crystal sensor has clear access to the inside of the shroud. Check the metal boats for cracks. Replace if cracks are visible.
4. Take one aluminum pellet and clean with IPA. Use tweezers to load one into each of the metal boats.
5. Close the shroud door.
6. Clean the O-ring gasket on the chamber using a clean glove. Clean the base-well using a wipe and IPA.
7. Lower the bell jar until it is seated on the sealing surface.

Pump Down

1. Close the foreline valve. The system will not allow any valve to change state until the valve is fully closed.
2. Open the roughing valve.
3. Monitor the foreline pressure. If it exceeds 30 mTorr, then
4. Close the roughing valve. The system will not allow any valve to change state until the valve is fully closed.
5. Open the foreline valve. Pump the foreline until the pressure is < 10 mTorr.
6. Close the foreline valve. The system will not allow any valve to change state until the valve is fully closed.
7. Open the roughing valve and continue pumping down the chamber.
8. When the chamber pressure reaches ~30 mTorr ($3x10^{-2}$), close the roughing valve.
9. Open the foreline valve.
10. Open the high-vac valve
11. Turn on the cold cathode gauge by pressing 'CCG' on the monitor.
12. Monitor the pump-down time. It should take ~35-45 minutes to reach a pressure suitable for evaporation.

Evaporation

1. When the chamber pressure reaches 10^{-6} Torr (as indicated by the cold cathode gauge), evaporation can begin.
2. Turn on the power switch to the Concordia ac power supply. A reading of ~4 Amps should appear immediately on the digital display.
3. On the IC6000 controller, press 'FLM#', then '4' to set up the system for Aluminum operation.
4. Press 'START'. The controller will go through several stages:
5. Ramp 1: increases current through filaments at a controlled rate.
6. Soak 1: allows aluminum to heat up.
7. Ramp 2: increases current through filaments to a level just below the evaporating point of the metal
8. Soak 2: allows aluminum to heat up..
9. After 'Soak 2', the controller will adjust the current to the filament to maintain a deposition rate of 15Å/second, as indicated at the top left of the IC6000 display. will show the evaporation rate in Angstroms/s, while the top right readout will show the total accumulated metal evaporated. The rate should be 10-15 Angstroms/s normally.
10. The IC6000 will deposit 2000 Angstroms of metal (as indicated in the top right of the display), then turn off the power supply.
11. Turn off the power switch to the Concordia ac power supply.

Bring to Atmosphere

1. Close the high-vac valve.
2. Turn off the cold cathode gauge by pressing 'CCG' on the monitor.
3. Open the vent valve.
4. When the chamber is at atmospheric pressure (~760 Torr), raise the bell jar.
5. Remove the wafers.
6. Replace the wafer covers.

Standby

To maintain cleanliness and minimize pump down times, the evaporator chamber must be returned to a high vacuum state. Follow the same procedures described above for pump-down.

Schematics

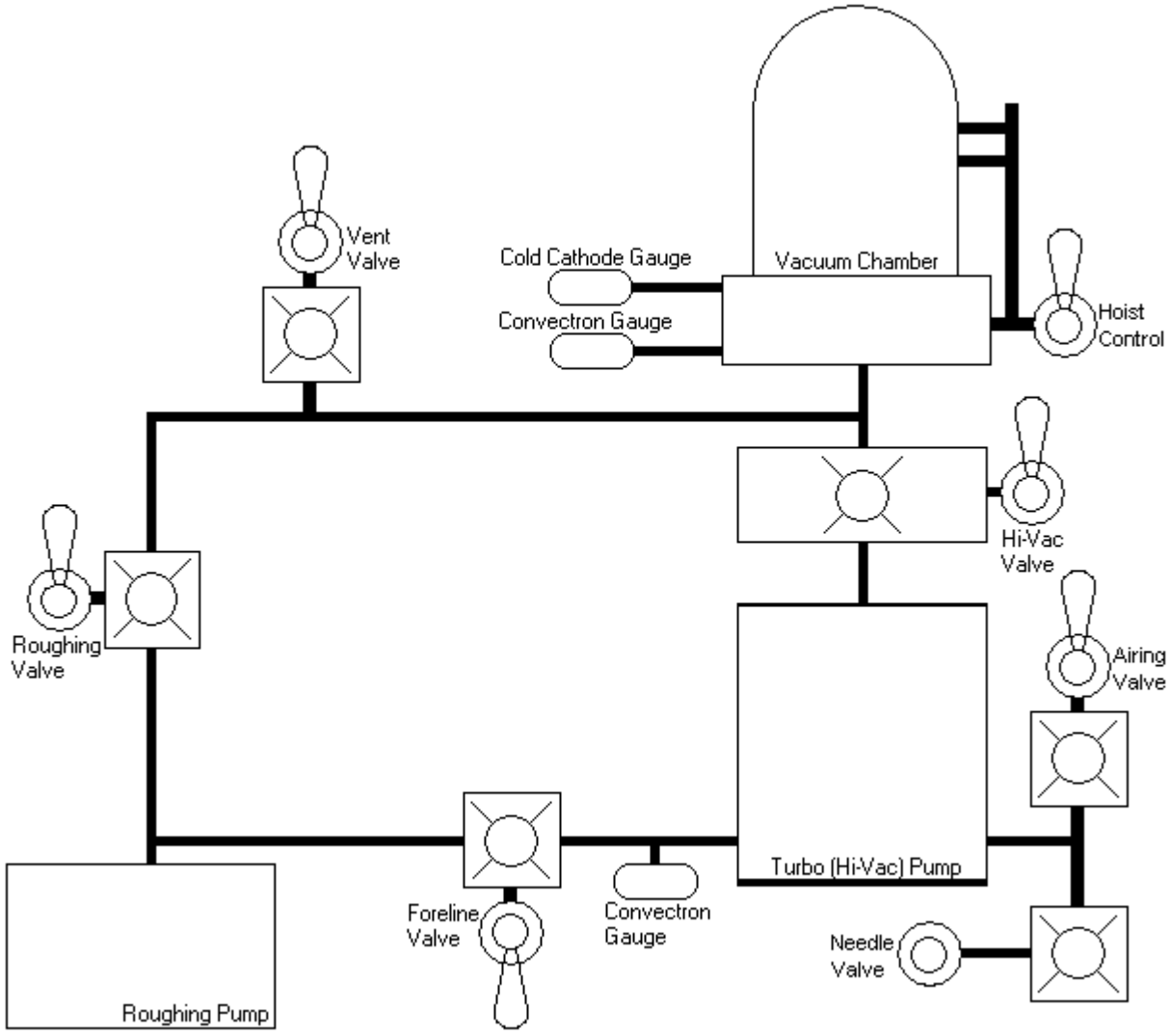


Figure 1: System Overview

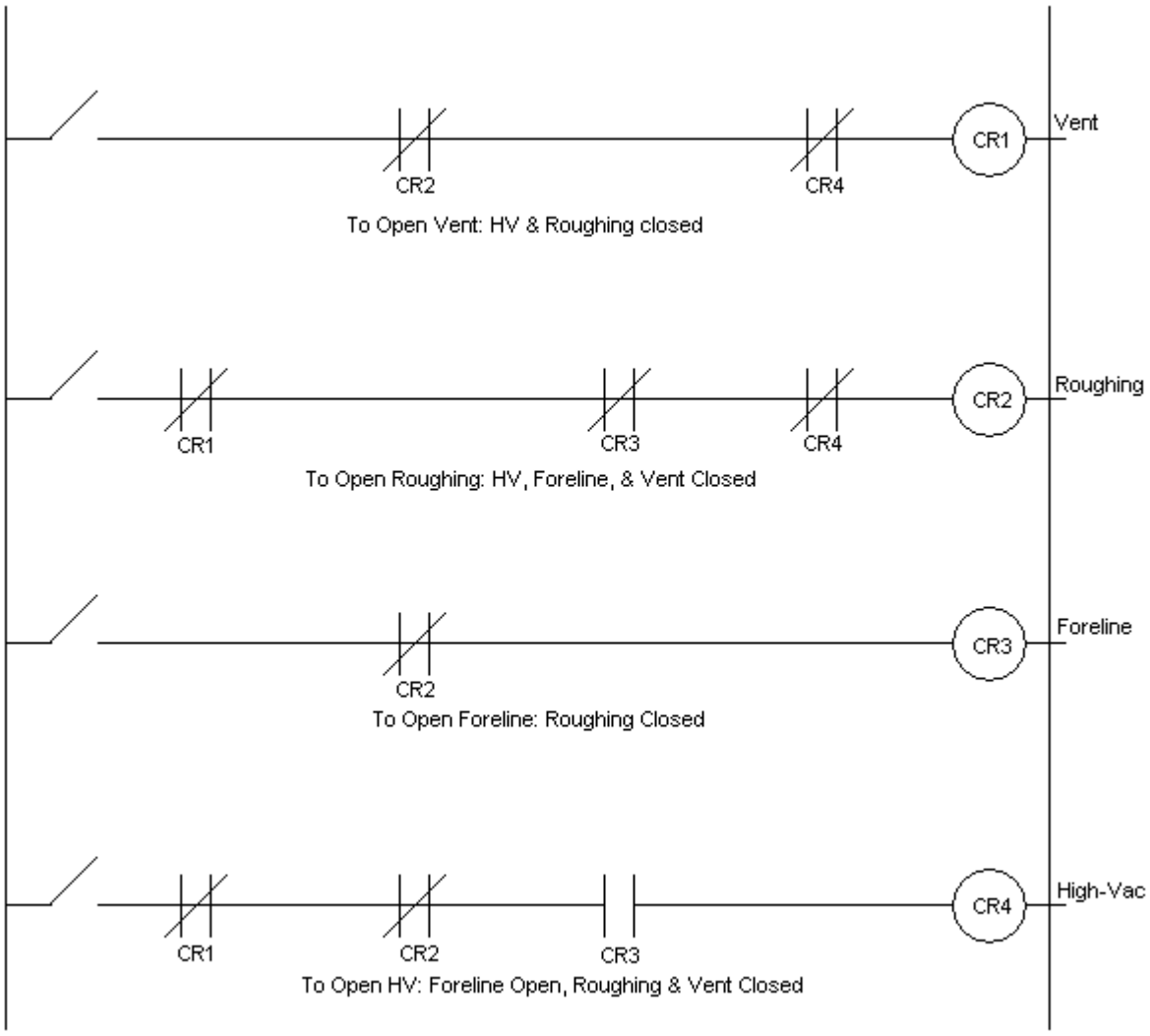


Figure 2: Ladder logic for valve relays

References

Leybold Vacuum, Inc., "Vacuum Technology: Its Foundations, Formulae and Tables", Ch. 2, 3.

www.helixtechnology.com, Vacuum Gauge Product Tour

MKS Instruments, "MKS Type 146A Vacuum Gauge Measurement and Control System Reference"

www.mksinst.com, Cold Cathode Sensor Product Page

www.leyboldvacuum.com, Leybold Turbomolecular pumps product page

Leybold-Inficon, "Leybold IC6000 Deposition Controller Manual"

Appendix C - Wafer Cleaning

Two methods are used for cleaning wafers in the ECE 444 lab. The first is simple degreasing. The other is the industry standard RCA clean.

Both procedures are posted in the wet lab area so you do not need to take your copy of this into the area. Not only is space limited, but paper is very dirty and dusty by semiconductor industry standards. There is no point in carefully cleaning a wafer if it is not kept in a clean environment. Use your individual wafer carriers to keep your wafer clean and safe from accidents after either of these cleaning procedures.

Degreasing Procedure*

The term degrease refers to the removal of the grime that often coats surfaces exposed to the atmosphere. The thin film is mostly organic in nature and is probably due to the presence of humans. 1,1,1 Trichloroethane (TCA) is particularly effective in dissolving this "grease" which is why it is commonly used in industry. Substitutes must be found, however, since compounds containing halogens (chlorine, fluorine, and bromine) are destroying our ozone.

Simple Degreasing

1. Hold wafer flat over the solvent waste container.
2. Squirt acetone over the front and back sides of the wafer.
3. Repeat step 1 using IPA.
4. Rinse wafer with DI water (either from the faucet or spray gun).
5. Repeat step 1 using IPA
6. Hold the wafer at a steep angle (~80°) and rest it against the drying block (make sure a clean wipe is covering the block).
7. Using the N_2 blow gun, start at the top of the wafer and 'chase' the IPA down the wafer. Repeat for the back side of the wafer. Alternate front and back until all moisture is gone. Make sure that the area under the tweezers is also dry.

Note: Acetone and IPA should be used over the "waste acetone and IPA" container. Always put the lid back on the waste container when finished.

Note: Acetone dissolves organic residue. IPA dissolves acetone residue and some residues not soluble in acetone. Water dissolves IPA residue and some residues not soluble in acetone or IPA. The final IPA rinse is only for making it easier to dry the wafer.

The RCA Clean

This cleaning method is the industry standard for cleaning wafers. Although every company has its own way of implementing the RCA clean, and many have introduced their own proprietary improvements, they have all been significantly influenced by the work of Kern, a chemist at RCA. One of his articles is included at the end of this appendix. Please read it. Below is the recipe for our particular implementation. We substitute sulfuric acid for hydrochloric acid as described in the other article at the end of this appendix. Ideally, if we had time, we would use this procedure before ***every*** diffusion furnace operation.

Preliminary Clean

Transfer the wafers to a Teflon wafer carrier specifically reserved for the RCA clean. This step is often performed while SC-1 is warming up.

1. Securely mount the Teflon wafer carrier handle, also reserved for the RCA clean.
2. The wafers should be degreased before continuing. The SC-1 solution can be prepared during the degreasing procedure.
3. Etch the wafers for 30 seconds in the 50:1 DI:HF etch.

SC - 1: Remove residual organics and certain metals using the RCA Standard Clean Solution 1

1. Rinse the quartz tub, temperature sensor and thermometer under the SC-1 hood.
2. Place the tub on the hotplate with the temperature sensor and thermometer inside.
3. Add 1800 ml of deionized water.
4. Turn on the temperature controller. It has been set for 75° C.

   NOTE: Whenever handling strong chemicals it is a very good idea to have DI slowly flowing from a faucet first. Not only will it help dilute accidental spills, but it allows you to rinse your gloves without getting the faucet valve contaminated. Always use the green nitrile gloves over the thin gloves when handling strong chemicals and rinse them afterward!
5. Slowly add 360 ml of 30% hydrogen peroxide.
6. Slowly add 180 ml of 58% ammonium hydroxide. Be sure to rinse the green nitrile gloves, the graduated cylinder, and the outside of the chemical containers with DI when finished.
7. Slowly stir the solution with a thermometer (don't break it!).
8. Slowly place the wafer carrier into the solution.
9. Occasionally stir the solution until it has been over 75°C for 10 minutes.
10. After the 10 minute clean, immerse the wafer carrier in the DI Rinse tank for 15-20 seconds.
11. Spray rinse the wafer carrier and as much of the handle as you can without getting your glove wet. Remember, at this point a drop of water from a relatively dirty glove could compromise the whole cleaning process.
12. Move the wafer carrier to the cascade rinse tank for at least 2 minutes.

NOTE: While waiting for the temperature to rise it is possible to begin preparation of the SC-2 solution. Do not forget to occasionally stir and check the temperature of the SC-1 solution!

Prepare SC-2 solution

1. Rinse the quartz tub, temperature sensor and thermometer under the SC-2 hood.
2. Place the tub on the hotplate with the temperature sensor and thermometer inside.
3. Add 1820 ml of deionized water.
4. Turn on the temperature controller. Verify that it is set for 80°C.
5. Slowly add 320 ml of 30% hydrogen peroxide.
6. Slowly add 110 ml of sulfuric acid.
7. Occasionally stir the solution with the thermometer.

8. When the solution has reached 75°C, continue.

Strip hydrous oxide

1. Move the wafer carrier to the 50:1 HF:DI tank for 15 seconds.
2. Agitate the carrier in the DI rinse tank for 20 to 30 seconds.

Desorb remaining contaminants

1. Place the wafer carrier in the hot SC-2 solution for 10 minutes.
2. Turn off the temperature controller.
3. Carefully move the wafer carrier to SC-2 DI rinse tank for 20 seconds.
4. Spray rinse the wafer carrier and as much of the handle as you can without getting your glove wet. Remember, at this point a drop of water from a relatively dirty glove could compromise the whole cleaning process.
5. Move the wafer carrier to the cascade rinse tank for 5 minutes. Kern recommended 20 minutes.

Dry the wafers

1. Rinse the special handle for lifting the wafer carrier from one end and switch it with the other handle.
2. Load the wafer carrier into the Verteq spin-rinse-dryer and press start.
3. Wait for the rinser dryer to stop by itself. Use the time wisely (e.g. prepare for the subsequent furnace operation).
4. Return the wafer carrier to the rinser-dryer after removing the wafers.
5. Clean and reorganize the area. If the next days' instructor discovers the telltale crystals of dried acid, your whole group will lose performance points.

Hydrogen peroxide solutions for silicon wafer cleaning – W. Kern

The "RCA Standard Clean" process is so well known throughout the semiconductor industry that many may not know its RCA origins. Further refinements are described in this article.

Abstract: *Clean silicon wafer surfaces suitable for device fabrication have been prepared successfully for nearly 20 years by the simple and safe sequential process described in this paper. The process is based on oxidation and dissolution of residual organic impurities and certain metal contaminants in a mixture of H_2o-NH_3OH-O_2O_2 at 75 to 80 °C, followed by dissolution and complexing of remaining trace metals and chemisorbed ions in H_2O-HCl-H_2O_2 at 75 to 80 °C. The effectiveness of the method was demonstrated originally by radioactive-tracer techniques, and was later confirmed by extensive analytical studies and device reliability tests.*

The RCA method has become widely accepted in the semiconductor industry. The original paper, published in 1970, is one of the most frequently cited publications in its field. The present report traces the development of the process since its origin in 1961, notes the supporting data from radioactive-tracer studies, and summarizes the essential facts underlying the effectiveness of the process. Additional information obtained more recently on the process and its implementation is briefly presented. An outline of the processing procedures that are now recommended has also been included.

Final manuscript received June 1, 1983
Reprint RE-28-4-9

The RCA method for chemically cleaning silicon wafers has become widely accepted in the semiconductor industry. The original paper[1] is one of the most frequently cited publication in its field, according to the *Science Citation Index*. The Institute for Scientific Information has requested a commentary on this work for publication in the "Citation Classics" section of *Current Contents*.[2] The present paper traces the historical development of the process since its origin in 1961, notes the supporting data from radioactive-tracer studies, and summarizes the essential facts underlying the procedures. An outline of the recommended processing procedures has been included in an accompanying box.

Need and requirements of a cleaning procedure

The work published in our 1970 article originated in 1961 at the RCA Solid State Division is Somerville, New Jersey, when it was realized that residual trace impurities on silicon surfaces prior to high-temperature processing - particularly diffusion, thermal oxidation, and epitaxial growth - can have detrimental effects on surface stability, reliability, electrical performance, and production yield of devices, especially sensitive metal-oxide-semiconductor types. It became clear to me that a highly effective yet simple and hazard free process was needed for purifying pre-cleaned silicon wafers, as well as thermally oxidized patterned or unpatterned wafers.

The procedures used up to that time involved hot mixtures of concentrated sulfuric acid and hydrogen peroxide, or of concentrated sulfuric acid and chromic acid. The first was suspected of causing sulfur contamination and was extremely hazardous when used by operators in a production environment. The second was suspected of leading to chromium contamination and posed serious ecological problems of disposal. Clearly, a procedure was needed that was effective, free of contaminants introduced by the reagents, safe, economical, and ecologically acceptable.

Chemical considerations

The new cleaning method to be developed had to first be based on first removing organic contaminants (such as grease films and photoresist residues masking the surface) to expose the wafer surface and render it hydrophilic ("water loving")., thereby rendering it accessible to aqueous chemical reagents. This step would then be followed by the removal of inorganic contaminants (such as trace metals and chemisorbed ions). Ideally, the reagents to accomplish these objectives had to be completely volatile and commercially available at high purity and low cost.

On the basis or reaction chemistry and reagent purity, water diluted, unstabilized hydrogen peroxide at high pH, attained by the addition of ammonium hydroxide solution appeared to be the ideal reagent for removing residual organic contaminants by oxidative breakdown and dissolution, if used at an elevated temperature for a suitable period of time. In addition, this solution would also remove several types of metals such as Cu, Ag, Ni, Co, Cd, and Au, due to complexing by the ammonium hydroxide.

For the second solution, I selected diluted hydrogen peroxide at low pH, prepared by adding hydrochloric acid solution. Used again at elevated temperature, this solution was to remove alkali ions and remaining metallic impurities. Displacement replating of heavy metals from solution would be prevented by the formation of soluble complexes with the resulting dissolved ions.

Deionized, distilled, and microfilterd water served as the diluent and rinsing agent. To prevent leaching of alkali and boron from Pyrex® (DuPont), and wafer holders of Teflon® (DuPont), and conducted systematic experiments for establishing optimal processing conditions and solution concentrations. Surface chemical analysis techniques and radioactive-tracer measurements served as very sensitive analytical methods for evaluating the efficiency of various cleaning processes in the course of this development.

The results of these experiments subsequently showed that the solution compositions are not critical for the effectiveness of the process, as long as one operates within volume ratios of 4:1:1 to 6:1:1 of H_2O, 30 w/w% H_2O_2, and 29 w/w% NH_4OH (as NH_3) for

the first mixture, and 4:1:1 to 6:1:1 of H_2O, 30 w/w% H_2O_2, and 37% HCl for the second mixture. Treatment periods of 10 to 20 minutes are sufficient. The solution temperature can be maintained at 75 to 85°C, but preferably should not exceed 80°C. A higher temperature would cause rapid decomposition of the hydrogen peroxide.

Radiochemical contamination and cleaning efficiency studies

Concurrent with these studies I investigated the origin, cause, type, and concentration of contaminants by adding trace quantities of radioactive cations (Na^{22}, Na^{24}, Au^{198}, Cu^{64}, Fe^{59}, Cr^{51}, Zn^{65}, Sb^{122}, Sb^{124}, Mn^{54}, Mo^{99}) and anions (F^{18}, Cl^{38}, I^{131}, C^{14} - organics) to numerous etchant and reagent solutions. Radioactivity measurements, autoradiography, and gamma-ray spectroscopy of electronic solids (Si, SiO_2, Ge, GaAs) treated with these tagged solutions allowed quantization of the resulting surface concentrations of specific impurities, both initially and after various rinsing and cleaning steps with the hydrogen peroxide mixtures noted.[3-8]

Application to silicon device production

By mid-1960, the peroxide cleaning technique (dubbed "SC-1" and "SC-2" to denote "Standard Clean, Solutions 1 and 2" - see box) was well established and widely applied at RCA in the fabrication of silicon devices. A process patent that incorporated the HCl-H_2O_2 desorption process was issued to RCA in 1966.[9] Also in 1966, I received an RCA Outstanding Achievement Award shared with James A. Amick and Arthur I. Stoller "for new technological advances for processing integrated circuits," which included the peroxide method for attatining practically clean silicon surfaces in conjunction with glass-passivation and tungsten-metallization processes.

Publications

In 1970 I succeeded in obtaining permission to publish the series of papers on the radiochemical studies and the peroxide cleaning process: the latter incorporated the contributions of my co-author, David A. Puotinen, who had studied in some detail several aspects of peroxide cleaning as applied to silicon device processing.

Several of my colleagues contributed also to the success of this work, particularly Norman Goldsmith and James A. Amick[10] during the development and implementation that extended over several years, and Alfted Mayer who introduced megasonic (ultrahigh-frequency) peroxide cleaning at low temperature (explained below), effectively combining the removal of particulates with the desorption of adsorbed contaminants.

Introduction of additional process step

An additional step in the procedure, which was not explicitly noted in our original paper because of insufficient data at that time, is the application of a brief etch in dilute HF solution after the SC-1 cleaning. I reasoned that removal of the hydrous oxide film formed during the SC-1 treatment to reexpose the silicon surface for the subsequent SC-2 desorption step should further increase the purification efficiency. However, this etching should be done with a very dilute high-purity HF solution and for a very short period of time to avoid replating of the metallic contaminants from the HF solution on the silicon surface.

Experiments have shown that a 10-second immersion in 1:50 HF-H_20 is sufficient to remove this film, as evidenced by the change of the hydrophilic oxidized surface to a hydrophobic surface, which is characteristic for a fluoridated, organic contaminant-free silicon surface. Subsequent water rinsing should also be kept very brief (30 seconds), serving only to remove HF solution from the wafer assembly in order to minimize regrowth of a new hydrous oxide film Fortunately, change of a ≡Si-F surface to a ≡Si-OH surface in cold H2O is very slow, minimizing rapid regrowth of a hydrated oxide film.[5] We believe that this additional step does indeed enhance the effectiveness of the subsequent SC-2 treatment, and should be part of the cleaning sequence.

Reasons for popularity of cleaning procedure

The original paper of 1970 has been highly cited because extensive analytical studies and device reliability and life testing by many independent researchers have confirmed the process, now widely known as "RCA Standard Clean," to be the most effective cleaning method known for attaining the degree of purity that is imperative in the fabrication of sensitive silicon semiconductor devices. Furthermore, the process is safe and relatively simple, has attractive economic and ecological advantages, uses readily available high-purity solid free and volatile reagents, and was accepted by the American Society for Testing and Material as a standard procedure.[12] Actually the process is so widely employed that most authors refer to it without citing our original work, apparently assuming it to be common knowledge.

Developments since 1970

The following section reviews the more important literature references on silicon wafer cleaning with SC-1 and SC-2 hydrogen peroxide solutions. These references confirm our original statements and contribute additional new information on the subject.

Henderson[13] published results in 1972 on the analytical evaluation of the SC-1/SC-2 cleaning process by high-energy electron diffraction and Auger electron spectroscopy. He concluded that the process is well suited for silicon wafer cleaning prior to high-temperature treatments, as long as quartzware is used for processing, according to our specifications, to avoid boron contamination from Pyrex® containers. He also examined the possible benefits of an additional final etch treatment in concentrated HF after completion of the SC-1/SC-2 steps, but found that it enhances carbon contamination and causes surface roughening during vacuum heating at 1100°C due to loss of the protective 15-angstrom thick carbonfree oxide film remaining after the SC-2 step. Reexposure of a bare silicon surface to HF after SC-2 would, of course, be ill advised because of recontamination with metallic impurities, obliterating the advantages of peroxide cleaning.

Meek *et al,* (1973)[14] investigated the removal of inorganic contaminants, including copper and heavy metals, from chemically/mechanically polished silicon wafers by several reagent solutions. Using Rutherford back-scattering with 2-MeV He^+ ions as an analytical tool, they concluded that the SC-1/SC-2 as preoxidation cleaning process always removed all elements heavier than chlorine to below the level of detectability. Sulfur and chlorine remained after either SC-1, SC-2, or other cleaning procedures

studied at levels of about 10^{13}/cm2. SC-1/SC-2 cleaning eliminated calcium and copper much more reliable than did HF-HNO3 treatments.

Murarka *et al,* (1977)[15] studied methods for oxidizing silicon without the formation of stacking faults. They concluded that chemical cleaning of the wafers with SC-1/SC-2 prior to an oxidation is an essential requirement to ensure the complete elimination of stacking faults after the high-temperature processing.

In 1978, we published a review[16] of the entire field of surface contamination and semiconductor cleaning techniques as part of a book chapter on the chemical etching of thin films and substrates.

Gluck (1978)[17] presented a paper in which he discussed the removal of radioactive gold from silicon wafers by a variety of baths containing H_2O_2, H_2O, NH_4OH, and/or HCl. The desorption efficiency of SC-1 solution was more effective than that of SC-2, but the usual sequential treatment of SC-1 followed by SC-2 was the most effective removal method at higher gold surface concentration (in the $10^{14}/cm^2$ range).

Peters and Deckert (1979)[18] investigated photoresist stripping b numerous solvents, chemical agents, plasma stripping, and heat treatment in air at 650°C (combustion, or ashing). They found that film residues remain on wafers in all cases except ashing. The SC-1 procedure was the only technique by which the residues could be removed consistently and completely. They recommended that SC-1 cleaning be applied routinely to SiO_2-patterned silicon wafers after photoresist stripping operations in oxide masking.

In a 1981 review article on wafer cleaning, Burkman[19] reported results of desorption tests for radioactive gold from silicon wafers with several reagent solutions. A centrifugal spray cleaning machine by FSI Corporation was used rather than bath immersion. An SC-1 type of H_2O-NH_4OH-H_2O_2 solution was much more effective than H_2SO_4-H_20 mixtures, but an H_2O-HCl-H_2O_2 solution alone showed poor efficiency, probably because an organic film masked the surface, thereby preventing efficient gold desorption.

Phillips *et al,* (1983)[20] applied, in preliminary tests, secondary ion mass spectrometry to determine the relative quantities of contaminants on silicon wafers. Cleaned wafers were purposely contaminated gross quantities of numerous inorganic impurities and then cleaned by immersion or spray techniques with various aggressive reagents (aqua regia,, hot fuming nitric acid, sulfuric acid-hydrogen peroxide, and SC-1/HF/SC-2 type of solutions). The lowest residual concentrations for most impurity elements were obtained by spray cleaning with a sulfuric acid and hydrogen peroxide mixture as used for photoresist stripping, followed by the SC-1/HF/SC-2 cleaning sequence.

Watanabe *et al* (1983)[21] measured the dissolution rate of SiO_2 and Si_3N_4 films in H_2O-NH_4OH-H_2O_2 mixtures. The etching rate of thermally grown SiO_2 in SC-1 (5:1:1 of H_2O-NH_4OH-H_2O_2) during a 20-minute treatment at 80°C was a constant 4 angstroms per minute. The authors state that this rate of dissolution is significant for structures incorporating thin (200 angstroms or so) oxide layers (one might argue that the processing of such layers should be designed to use as-grown films to make chemical treatments unnecessary). The etch rate of high-temperature chemically vapor-deposited Si_3N_4 was 2 angstroms per minute under the same conditions.

Measurements done in 1981 in the author's laboratory at RCA, however, indicated much lower oxide-dissolution rates under nearly identical conditions. Changes in film thickness were measured by ellipsometry after each of four consecutive treatments in fresh 5:1:1 SC-1 at 85°C and totaled only 70 angstroms per 80 minutes, or 0.9 angstroms per minute, whereas in solution without peroxide (1:6 H_2O-NH_4OH) the rates were 1.6 angstroms per minute. Under the same conditions, 6:1:1 SC-2 solution showed practically no change in the film thicknesses, as would be expected.

Alternative processing techniques using SC-1/SC-2

The original and widely used RCA cleaning procedure is based on simple immersion techniques. Two alternative and attractive techniques have been introduced in recent years: centrifugal spray cleaning[19] and megasonic cleaning[11,12].

In centrifugal spray cleaning, developed by FSI Corporation, the wafers are enclosed in a chamber purged with nitrogen. A sequence of continuous fine sprays of reagent solutions, including hot SC-1, SC-2, and high-purity water, wets the spinning wafers; N_2 finally dries them for removal. The main advantages of this automated system are the reduced volume of chemicals needed, the continuous supply of fresh reagent solutions to the wafer surface, and the controlled environmental conditions during the processing. The cleaning efficiency of the centrifugal spray system is comparable with that obtained with the RCA immersion technique, according to claims by FSI Corporation.

The megasonic cleaning system was patented in 1975 by RCA Corporation[11,12] and is manufactured under license by the Process System Division of Fluorocarbon Company. It is a noncontact, brushless scrubbing machine designed primarily for safely removing particulate contaminants from both sides of silicon wafers by use of ultrahigh-frequency sonic energy. Sonic waves of 85 kHz are generated by an array of piezoelectric transducers, providing a highly effective scrubbing action on batches of wafers immersed in the cleaning solution. Particles ranging in size from several micrometers down to about 0.3 μm can be efficiently removed with input power densities of 5 to 10 W/cm^2. For comparison, ultrasonic systems that operate typically at 25 to 80 kHz require power densities of up to 50 times that of the megasonic system, and are much less effective for removing very small particles.

An interesting additional aspect of this machine is its ability to operate effectively with SC-1 and SC-2 cleaning solutions for the removal of organic and many inorganic contaminants, similar to the RCA immersion technique, even though the bath temperature rises to only 35 to 42°C during operation. Initial experimental data of desorption efficiencies for metallic and ionic contaminants are impressive, but an extensive and quantitative evaluation has not yet been carried out to assess the extent of effectiveness. At present, any degree of chemical cleaning and desorption of contaminants resulting simultaneously with particle removal, the main function intended of the machine, can be considered a highly desirable additional benefit of this system. Photographs of a typical machine are shown in Figs. 1a and 1b.

Comments and recommendations

It is important to stress that the wafers during processing must never be allowed to dry, because dried residues may be difficult to redissolve and may mask the surface during subsequent treatments. Removal from a hot bath should therefore be done only after cooling or quenching the solution by dilution with cold water. This technique also minimizes contamination from the solution/air interface.

Vapors of NH_3 and HCl form a smog of NH_4Cl when brought in close proximity to each other. Therefore, the SC-1 must be separated from the SC-2 processing by the use of two separate exhaust hoods to avoid wafer contamination from colloidal NH4Cl particles. Disregard of this recommendation has repeatedly led to problems in production application.

Pyrex® glassware should not be used with the SC-1 and SC-2 procedures because substantial amounts of sodium, potassium, boron, and impurities are leached out of the glass by the hot solutions. As noted, beakers of fused silica should be used instead; high-quality opaque fused silica is much less costly than clear fused quartz, and is acceptable for wafer-cleaning vessels. Rinse tanks and vessels for HF solution should be constructed of high-grade polypropylene plastic.

Operators frequently believe that if hot SC-1 solution is good for processing, a boiling solution must be better. This fallacy is remarkably difficult to correct. As noted, the solutions, especially the SC-1, should be used at a temperature in the range of 75 to 80°C because, at higher temperatures, H_2O_2 rapidly decomposes and there is increased volatilization of NH_3 from the NH_4OH solution. Fortunately, for SC-1 solutions the rate of H_2O_2 decomposition and of NH_3 volatilization under the recommended processing conditions are similar; ammonia in the absence of H_2O_2 would immediately etch silicon. In the case of SC-2 solutions, the decomposition of the H_2O_2 and volatilization of HCl proceed at much slower rate than for SC-1, and there is no danger of silicon etching under any conditions. Nevertheless, excessive heating should be avoided for safe operation.

To illustrate the degree of decomposition of hydrogen peroxide in an SC-1 solution as a function of extreme temperature and time conditions, the graph from our original paper[1] is reproduced in Fig. 2. It can be seen that the half-life of the solution at 88 to 90°C was approximately 5 minutes (versus 50 hours at 23°C), and the time for the concentration of peroxide to be reduced to the etching threshold level for (111)-orientated silicon was more than 40 minutes after the solution reached 79°C. Since the preferred recommended cleaning time is minutes at a temperature of 75 to 80°C, there is an adequate margin of safety if the initial peroxide concentration is at the recommended level. Recent measurements, which we conducted with SC-1/SC-2 reagents that are now available at much higher purity than before 1970, have shown considerably lower rates of decomposition.

A wide range of SC-1 and SC-2 compositions has been used successfully by many engineers. The recommended ratios of 5:1:1 for H_2O-NH_4OH-H_2O_2, and of 6:1:1 for H_2O-HCl-H_2O_2, are effective and economical ratios used by most people. Repeated use of the solutions, or reconstitution of the reagent composition, is not recommended because it would prevent the safe technique of overflow-quenching with cold water. Besides, impurities accumulate in the solutions and accelerate the decomposition rate of H_2O_2.

The use of unstabilized H_2O_2, that is H_2O_2 without stabilizer additions, has been specified. Principal additives in commercial stabilized H_2O_2 are sodium phosphate and or sodium stannate, compounds that are highly undesirable contaminants in our application.

Occasionally, etching of silicon areas in device wafers during SC-1 cleaning has been encountered. The most likely explanation for this effect is a catalytically accelerated decomposition of the H_2O_2 due to trace impurities, especially heavy metals from tweezers or containers, or impurities in the reagents. Decomposition may then take place even at a low temperature, or on mixing of the solutions. In the absence of sufficient quantities of H_2O_2 (initial concentrations of less than 50 percent of what we recommend), the ammonium hydroxide will etch silicon at rates dependent on crystallographic orientation, dopant types and concentrations in the silicon, and proximity of *p*- and *n*-type areas.[1] The light intensity during this treatment may also be a factor. A detailed outline of the exact, updated processing procedures that are recommended is presented in the accompanying box.

Acknowledgment

I wish to thank Richard E. Berger for carrying out the experimental work and measurements, Stanley Shwartman for providing the megasonic system photographs, and George L. Schnable for reviewing the manuscript and making valuable comments.

References

1. W. Kern and D.A. Puotinen, "Cleaning Solutions Based on Hydrogen Peroxide for Use in Silicon Semiconductor Technology," *RCA Review*, Vol. 31, pp. 187-206 (1970)
2. W. Kern, "Use of Radioisotopes in the Semiconductor Field at RCA," *RCA Engineer*, Vol. 9, No. 1, pp. 62-68 (1963)
3. W. Kern, "Cleaning Solutions Based on Hydrogen Peroxide for use in Silicon Semiconductor Technology," Citation Classic, *Current Contents, Engineering, Technology, and Applied Sciences*, Vol. 14, No. 11, p. 18 (March 14, 1983)
4. W. Kern, "Radioisotopes in Semiconductor Science and Technology," *Semiconductor Products & Solid State Technology*, Vol. 6, No. 10, pp. 22-26: No. 11, pp. 23-27 (October and November 1963)
5. W. Kern, "Radiochemical Studies of Semiconductor Contaminations - I. Adsorption of Reagent Components," *RCA Review*, Vol. 31, pp. 207-223 (1973)
6. W. Kern, "Radiochemical Studies of Semiconductor Surface Contamination-II. Adsorption of Trace Impurities," *RCA Review*, Vol. 31, pp. 234-264 (1970)
7. W. Kern, "Radiochemical Study of Semiconductor Surface Contamination-III. Deposition of Trace Impurities on Germanium and Gallium Arsenide," *RCA Review*, Vol. 32, pp. 64-87 (1971)
8. W. Kern, "Semiconductor Surface Contamination Investigated by Radioactive Tracer Techniques," *Solid State Technology*, vol. 5, No. 1, pp. 34-38; No. 2, pp. 39-45 (January and February 1972)
9. J.A. Schramm, "Method of Fabricating a Semiconductor Device," U.S. Patent No. 3,281,915 (November 1, 1966)
10. J.A. Amick, "Cleanliness and the Cleaning of Silicon Wafers," Solid State Technology, Vol. 47, No. 11, pp. 47-52 (November 1976)
11. A. Mayer and S. Shwartzman, "Megasonic Cleaning: A New Cleaning and Drying System for Use in Semiconductor Processing," *J. Electronic Materials*, Vol. 8, pp. 855-864 (1979)
12. "Standard Test Method for Detection of Swirls and Striations in Chemically Polished Silicon Wafers," ASTM F416-77; *Annual Book of ASTM Standards*, Part 43, Electronics, American Society for Testing and Materials, Philadelphia, Pa., pp. 840-851 (1981)
13. R.C. Henderson, "Silicon Cleaning with Hydrogen Peroxide Solutions: A High-Energy Electron Diffraction and Auger Electron Spectroscopy Study," *J. Eletrochem. Soc.*, Vol. 119, pp. 772-775 (1972)
14. R.L. Meek, T.M. buck, and C.F. Gibbon, "Silicon Surgace Contamination: Polishing and Cleaning," *J. Electrochem. Soc.*, Vol. 120, pp. 1241-1246 (1973)
15. S.P. Murarka, H.J. Levinstein, R.B. Marcus, and R.S. Wagner, "Oxidation of Silicon Without the Formation of Stacking Faults," *J. Applied Physics*, Vol. 48, pp. 4001-4003 (1979)
16. W. Kern and C.A. Deckert, "Chemical Etching," Part V-1, *Thin Film Processes*; J.L. Vossen and W. Kern, Editors, Academic Press, New York, N.Y., pp 411-413 (1978)
17. R.M.Gluck, "Gold Removal from Silicon with Dilute Peroxide Mixtures Containing NH_4OH and/or HCl," *Electrochem. Soc. Ext. Abstr*, 78-2, 640, Abstract No. 238 (1978)
18. D.A. Peters and C.A. Deckert, "Removal of Photoresist Film Residues from Wafer Surfaces," *J. Electrochem. Soc.*, Vol. 126, pp. 883-886 (1979)
19. D. Burkman, "Optimizing the Cleaning Procedure for Silicon Wafers Prior to High Temperature Operations," *Semiconductor International*, Vol. 4, No. 7, pp. 103-116 (July 1981)
20. B.F. Phillips, D.C. Burkman, W.R. Schmidt, and C.A. Peterson, "The Impact of Surface Analysis Technolgy on the Development of Semiconductor Wafer Cleaning Processess," *J. Vac. Sci. Tech.* Vol. A1, No. 2, pp. 646-649 (1983)
21. M. Watanabe, M. Harazono, Y. Hiratsuka, and T. Edamure, "Etching Rates of SiO_2 and Si_3N_4 Insulating Films in Ammonia Hydrogen-Peroxide Cleaning Process, " *Electrochem. Soc. Ext. Abstr.*, Vol. 83-1, pp. 221-222, Abstract No. 139 (1983)

22. S. Shwartzman and A. Mayer, "Megasonic Cleaning of Surfaces," to be published in *Treatise on Clean Surgace Technology*, Vo. III, K.L. Mittal, Ed., Plenum Publishing Corporation, New York, N.Y. (1983)
23. J.R. Zuber and A.J. Gaska, "Elimination of Impurities from Silicon Discs," U.S. Patent No. 563,104 (March 28, 1975)
24. W. Kern, "A Technique for Measuring Etch Rates of Dielectric Filsm," *RCA Review*, Vol. 29, pp. 557-565 (1968)

Keeping the 'RCA' in Wet Chemistry Cleaning

-Taken from *Semiconductor International*, pp. 86-89, June 1994

Engineers will continue to tweak RCA wet chemistry formulae; it is unlikely that this, perhaps the most durable wafer processing technique, will be replaced en masse anytime soon.

Pieter Burgrgraaf
Senior Editor

Key Technologies:

- *Chemicals*
- *Wafer Cleaning Equipment*

At A Glance:

Ever since 1965, wafer processing operators have been mixing hydrogen peroxide with ammonium hydroxide and hydrochloric acid - the reagents in the infamous RCA clean. And since then, engineers, while marveling at the capabilities of these mixtures, have experimented with the recipes to improve the results or to keep their capabilities equal to the increasing demands of wafer processing. It is somewhat amazing that today the RCA formulae are still the basis of wet chemistry cleaning in virtually all wafer processing operations worldwide. In various easily recognizable forms, often with an additional step or two added, many experts foresee hydrogen peroxide-based wet cleans meeting the industry's needs through the turn of the century. Yet there are suggested alternatives to this technology, its relatively high cost being perhaps the driver for change.

Hydrogen peroxide-based "RCA" wet cleans still dominate in wafer processing. Researchers have tweaked the mixtures and procedures over the years so that current recipes are just as capable of cleaning today's wafers as Werner Kern's original recipes (Table 1) were in cleaning wafers in 1965 at RCA1. John Rosato, Ph.D., R&D manager at Santa Clara Plastics, says, "They continue to be the cleans of choice for most pre-furnace applications, particularly for critical steps such as gate oxidation."

Tweaking the chemistry

Certainly, much of the success of wet chemistry wafer cleaning must be attributed to today's high purity reagents that go into the RCA formulae. Werner Kern, Werner Kern Associates (East Windsor, N.J.), notes, "High purity chemicals, including aluminum free H2O2, low particulate HF, and low metal HCl and NH4OH solutions have led to much lower trace metal contamination levels than were previously possible."

Today it is not uncommon to find RCA wafer cleaning done with a variety of sequence and mixture modifications. Rosato explains, "These often include adding to or changing the order of the basic SC-1 and SC-2 cleaning steps. For example, 'piranha' (98% H2SO4 and 30% H2O2) and HF steps may be used before, after or between the SC-1 and SC-2 steps. Ending the sequence with an HF-last step is common for chemical vapor deposition and pre-metalization processes." In other cases, either the SC-1 or SC-2 step may be deleted, depending on critical needs for a particular process.

Work on the HF-last step at the Interuniversity Micro-Electronics Center (IMEC, Leuven, Belgium) has shown that HF-dipping time must be optimized to obtain a highly passivated surface that is resistant to particle recontamination. IMEC engineers have also shown that the addition chloroacetic acid to dilute HF solutions result in excellent metal removal properties (use of "chelating agents" are discussed later in this article).

Other work has shown that surfactant additives, such as isopropyl alcohol, can lower the surface-free energy and increase surface passivation. For example, research by Dr. Tadahiro Ohmi at Tohoku University (Sendai, Japan) has found that surfactants in HF improve the wetting of hydrophobic silicon and help prevent particle adhesion.

Suggestions for more dramatic RCA clean sequence and mixture modifications have also come out of work at IMEC: Reporting at the May 1994 IES Conference in Chicago, IMEC engineers said that the standard SC-2 solution can be replaced with dilute 0.1 mol/liter HCl without H2O2. This cuts chemical consumption and cost, while maintaining metal removal efficiency.

The idea that an HF-only or simplified RCA recipe can significantly cut the cost of wet cleaning is a paramount consideration for future semiconductor manufacturing. Chris McConnel, president of CFM Technologies, notes that systematic investigations of time, temperature, reagent strength and acoustic energy have led to optimized RCA cleaning recipes. "Along with enhancements in cleaning performance, some of these studies have led to startling reductions in cost-of-ownership; for example, an IBM study co-sponsored by CFM and SEMATECH demonstrated a nearly ten-fold reduction in chemical consumption. Other savings come with overall throughput improvement and total cost per wafer pass," he says.

Certainly, the chemical cost side of wet cleaning will continue to be addressed: J.T. Baker (Phillipsburg, N.J.), for example, has an emerging product with the code name "Dublin" slated for formal introduction in July 1994: it's described as "an aqueous-based chemical replacement for the RCA clean." Baker's Mike Thompson reports, "While 'Dublin' is still under beta site evaluation to correlate yield and electrical improvements corresponding to improved trace impurity and particle removal as well as improved

microroughness, the significant advancement may be its reduction in processing time ad the volume of liquid required for wet processing."

Microroughening

Because the SC-1 step cleans particles and some trace metals by continuous chemical growth and etching of a hydrous oxide film on silicon, it is known that the standard 5:1:1 solution can cause microroughening of any exposed silicon in a circuit pattern. Since the pioneering work by Ohmi, this problem has received much attention in the literature; in one study, researchers at IBM, CFM and SEMATECH used atomic force microscopy to observe bump-like microroughening caused by bubbles that blocked the surface reaction of SC-1 chemistry.

Other work by Ohmi, and organizations like IMEC, has shown that the NH_4OH:H_2O_2 ratio and the temperature of the SC-1 bath have to be optimized to balance the etching action of the solution and control microroughening, as well as particle removal efficiency. The current trend is to reduce the NH4OH concentration in SC-1 by altering the mixture ratio to 5:1:0.01-0.25. IMEC engineers also found that the chemicals used in this step have to be ultraclean to avoid problems with the decomposition of hydrogen peroxide that is triggered by iron and copper impurities at part per billion levels. IMEC's Marc Heyns says, "Such work is an excellent illustration of how a good understanding of the basic physico-chemical mechanisms involved is essential to develop cleaning recipes for the deep submicron technology era."

The process temperature of SC-1 chemistry is also crucial. James Milinaro, senior vice president at SubMicron Systems, says, "The ammonia concentration, therefore cleaning effectiveness, depletes at an alarming rate for higher process temperatures." He advocates point-of-use ammonia concentration monitoring to lengthen SC-1 clean effectiveness and utilization.

Systems with automatic chemical fill capabilities can also help to control reagent strength and thereby counter the unavoidable degradation of hydrogen peroxide and evaporative losses of NH_4OH and HCl. McConnel notes, "More sophisticated systems include on-line instrumentation to measure chemical composition in real-time."

In other work, Michael Olesen, process engineering manager at Verteq Process Systems, reports that megasonic energy, along with chemistry dilution, helps to remove sub-0.2μm particles without increasing surface roughness.

Molinaro adds that high power acoustics (400-800 W) allow the SC-1 and SC-2 chemistries to operate at lower temperatures. Lower temperatures mean lower metallic contamination and lower etch rate with SC-1, and higher particle removal efficiencies.

Indeed, studies at Sandia National Laboratory (Albuquerque, N.M.) and Santa Clara Plastics have shown that acoustic energy can be used to balance the "low temperature and concentration" requirements for controlling microroughening with the "high temperature and concentration" requirements for particle removal efficiency.

In addition to the reduction of microroughening and associated improvements in device performance, Kurt Christenson, Ph.D., senior process physicist at FSI International, sees other benefits for pursuing dilute blend ratios in RCA cleans: "Because DI water is normally much purer that the chemicals used, one way to improve the purity of your process chemistries is to further dilute them with pure water."

Equipment costs issues

Increasingly, the cost savings associated with wet chemistry wafer cleaning are directly related to the equipment set (Table 2) used to implement a clean:

The trend with wet bench systems for immersion processing is smaller process vessels with "cassetteless" operation and fully robotic wafer handling within a minienvironment. Here the advantages include a substantial reduction in chemical consumption and shorter rinse times. These factors generally increase overall throughput, reduce equipment footprint, and lower the cost f ownership. Clearly, the cassetteless concept has helped change wet benches from expensive, time consuming systems that occupy enormous cleanroom space. For example, Rosato explains that Santa Clara Plastics reduced wet bench footprint by changing from the standard "poly" boat to a reduced cassette design. "The use of minienvironments also reduces exhaust costs and relaxes the requirements for the cleanroom," he says.

The capabilities of spray acid wet processing also has resulted in savings. Brian Gardner, manger of the applications laboratory at Semitool, says, "Once considered too expensive, spray processors are now very cost-effective alternatives to conventional wet bench technology when considering price, footprint, chemical consumption and facilities requirements." For future applications, Semitool is developing an automated high throughput batch cassetteless processor featuring both spray and immersion technology. FSI's Christenson notes that the work of Ohmi has demonstrated significant improvements in metallic and organic contamination removal when using spin-spray cleaning techniques.

Use of ozone

Ozone has been used by a few semiconductor manufacturers as a replacement for H_2O_2 in piranha cleans since the early 1980s; the advantages are a stronger oxidizing effect and a reduction in metallic contamination associated with liquid chemicals. Several researchers have suggested that ozone injected into DI water can replace a piranha step used for light organic cleaning; here again, the main driving force is reduction in chemical costs along with lower chemical waste.

Some cleaning researchers are suggesting that ozone can be more widely applied. Indeed, McConnell state that from the results of a literature survey, CFM has concluded that ozone has good potential for oxidizing noble metals in the SC-2 step, but that its very short half-life and low solubility in alkaline solutions precludes its use for growing silicon dioxide in the SC-1 step.

Chelating agents?

There is an older technique that may find new use: Adding a chemical chelating agent, such as ethylenediaminetetra-acetic acid (EDTA), to a cleaning solution to bind and remove metallic ions as a soluble coordination compound was developed by Werner at RCA in the late 1960s. More recently, this technique has been investigated by Ohmi and other Japanese engineers and is likely being used in Japan.

David Bohling at Air Products and Chemicals (Allentown, Pa.) explains, "As critical contamination thresholds diminish, the need for chelating agents in wet clean solutions will increase." Bohling explains that chelating agents can reduce redeposition of metals in solution, both by altering the reduction-oxidation potential of the metallic species and by reducing the chemical activity of

the species through chelation. "Metal chelate complexes are soluble in the various wet cleaning baths as discrete complexes. Equilibrium binding constants for this chelation effect are huge," he says. Good results using organic chelating agents, as has been done at IMEC, should make engineers look more positively on this technique.

Where from here...

In the past RCA cleaning was a "cook-book" recipe; today wet chemistry is truly a science. CFM's McConnell lists the achievements of this science: "Today we understand the fluid mechanics of interfacial phenomena such as droplets and bubbles. We have calculated the contributions of various particle adhesion forces. We have mechanistic models for various reactions including F etching. We can measure and predict surface roughness from excessive SC-1 treatment and from dissolved oxygen attack on bare silicon. We can quickly measure and control extremely low levels of metal contamination using analytical techniques, and we have a better understanding of adsorption and desorption equilibria for various ionic and metallic species."

The challenges left for wet chemistry cleaning include a further reduction of metallic and particle contamination, and improved rinsing efficiency. Enhanced drying techniques will also be needed, along with a better understanding of water spots an their deleterious impact between films. Greater understanding of gate-oxide growth is need as well, especially relative to hydrogen terminated silicon surfaces. Rosato says, "One of the biggest issues for wet processing is to achieve a controlled chemical bonding state." Wet chemistry process costs, while not part of the science, are also a challenge, perhaps the challenge through the end of the century: Users interviewed by Semiconductor International stress the importance of reducing chemical and DI water consumption, and increasing equipment utilization. The solutions will likely come from creative combination of chemistry an equipment engineering.

Some researchers have suggested that the future lies with an alternative wet chemistry cleaning technology. The most commonly referenced possibilities are:

HF-based cleaning - HF-last or HF-only cleans result in low metallic contamination, a hydrophobic hydrogen-terminated oxide-free surface, and a reduction in the number of cleaning steps required, meaning higher throughput and lower costs. HF, especially reprocessed HF, can be one of the cleanest chemical available.

Sulfuric-based cleaning - IMEC's proposal is for an H_2SO_4-H_2O_2 step followed by an HF step; among other advantages, this combination yields a native oxide-free surface, eliminates surface roughening, drastically reduces metallic contamination, and lowers processing costs. This clean may also benefit from acid reprocessing technology.

So far, however, most users are reluctant to stray too far from proven RCA formulae. The consensus among experts is that the RCA clean, in its various forms, will continue to see extensive use in production lines manufacturing devices down to 0.35μm - and even 0.25μm and beyond. Rosato says, "Most development work on quarter micron devices has already been demonstrated using standard wet cleaning techniques."

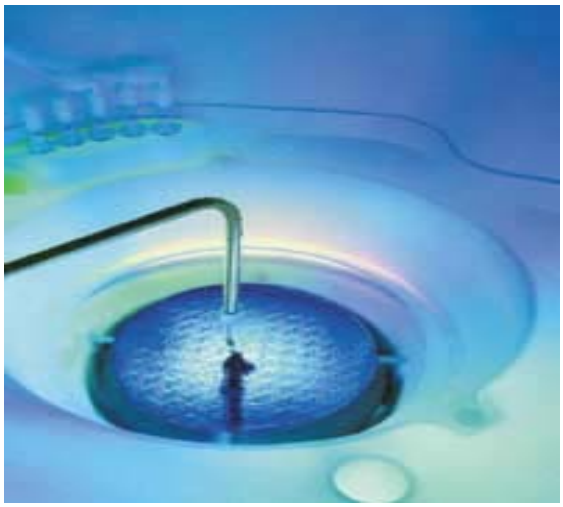
What is more likely is a change in dominance of conventional wet bench equipment sets for implementing RCA-based cleaning, especially as 300 and 400 mm wafers are used in production. Spray technologies offer a way around the high chemical and water use required for larger diameter wafers.

Reference

Kern, Werner, ed., Handbook of Semiconductor Wafer Cleaning Technology, Noyes Publications, N.J., 1993.

Single-Wafer, Short Cycle Time Wet Clean Technology

Steven Verhaverbeke, Satheesh Kuppurao, Christopher Beaudry and J. Kelly Truman,
Applied Materials Inc., Santa Clara, Calif.
7/1/2002 Semiconductor International



Applied Materials' 300 mm single-wafer Oasis Clean, with new chemistry and megasonics clean technology, removes virtually 100% of front and backside particles in <30 sec.

Wet chemical cleaning has been the work- horse in the semicon- ductor industry for more than 30 years. In 1965, Werner Kern and David Puotinen performed the first systematic study on the wet chemical cleaning of silicon surfaces, which was published in 1970.[1] This approach proved to be so successful that the industry adopted it. Even now, after 30 years, so-called RCA cleaning — named after the company where Kern and Puotinen developed this process — is still widely used. Other cleaning processes recently have been proposed — the IMEC clean,[2] Ohmi clean[3] and DDC clean[4] — but each of these processes had serious limitations and did not offer a substantial advantage over conventional RCA-type cleaning.

Applied Materials' 300 mm single-wafer Oasis Clean, with new chemistry and megasonics clean technology, removes virtually 100% of front and backside particles in <30 sec.

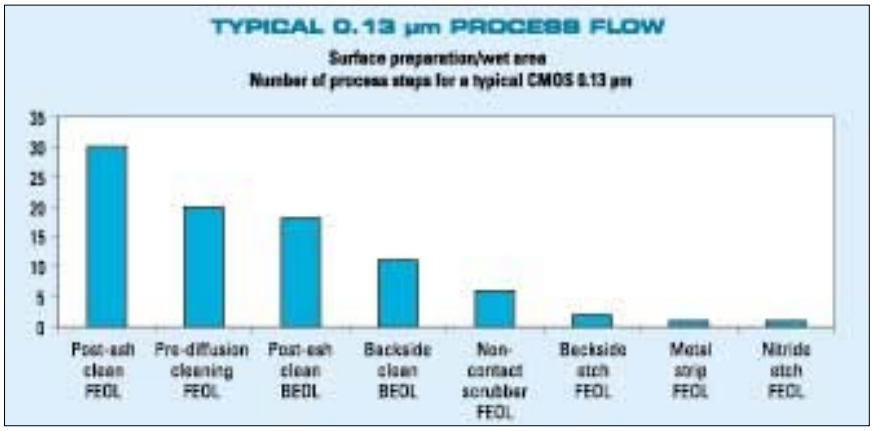
A typical RCA-type cleaning sequence consists of two steps. The first step, which is often referred to as the standard clean 1 or SC1, consists of an immersion in a bath of $NH_4OH/H_2O_2/H_2O$ for ~10 min. This step is mainly aimed at removing particles and organic contamination. The second step, which is often referred to as standard clean 2 or SC2, uses a mixture of $HCl/H_2O_2/H_2O$ for ~10 min. This step primarily is aimed at removing metallic contamination, often deposited during the SC1 step.

At a Glance
Using a new short cycle time wet cleaning technology, a typical >1 hr HF-SC1-SC2 process can be reduced to <2 min. The new system consists of horizontal single-wafer spin processing modules with novel full-coverage megasonics.

In a typical 0.13 µm logic flow, there are about 54 cleaning steps in the front end of line (FEOL) and 45 cleaning steps in the back end of line (BEOL).[5] This is illustrated in Figure 1 . The pre-diffusion cleans (20 steps) and the post-ash cleans (30 steps) typically include some variant of the RCA cleaning process. With smaller device geometries, the number of cleaning steps increases and is reaching >100 steps in some recent process flows. Increasing the number of cleaning cycles contributes to additional cycle time, cumulative silicon and oxide loss, and damage to fragile structures. Therefore, a shorter, more efficient cleaning process is critical to achieving high-productivity device manufacturing.

Single-wafer processing

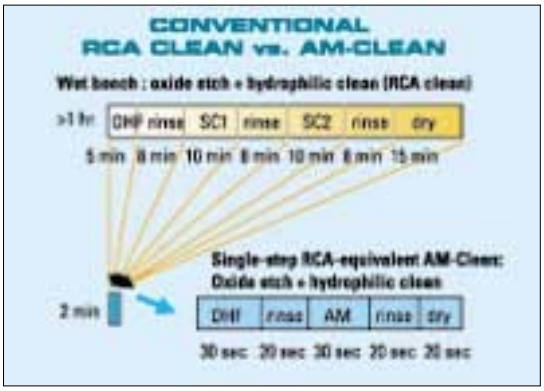
Single-wafer thermal processing techniques increasingly have been adopted in favor of more traditional batch systems because of technical performance, ease of integration with other technologies, and a dramatic reduction in production cycle time that enables customers to bring products to market more quickly.



1. Typical wafer cleans required in a 0.13 µm CMOS process flow, with about 54 cleans required for just front-end processing.

With the advent of 300 mm processing, batch wet clean systems pose increased risk of cross-contamination during critical cleans because of the decreased pitch between wafers and chemical recycling. Process constraints imposed by advanced devices (<0.13 µm) also restrict the amount of etching required by batch systems to obtain the high levels of particle removal and surface cleanliness. Single-wafer processing eliminates these hurdles and enables better technical performance for fine geometries. A single-wafer system also can reduce DI water consumption per wafer by an order of magnitude (10×) over batch systems.

One benefit of single-wafer wet processing is the potential to integrate it with complementary technologies. In the case of wet clean, its integration with gate dielectric deposition can control the surface condition for every wafer and reduce process variability. In addition, advanced gate dielectrics may require a variety of surface treatments under controlled conditions (e.g. ambient-controlled) that are possible only in a single-wafer mode. Also, integration of wet clean with dry photoresist-strip processes enables rapid turnaround and easy queue management in a fab, as well as reduced risk of particle growth between the strip and clean processes.



2. New approach reduces the cycle time of HF-SC1-SC2 from >1 hr to 2 min.

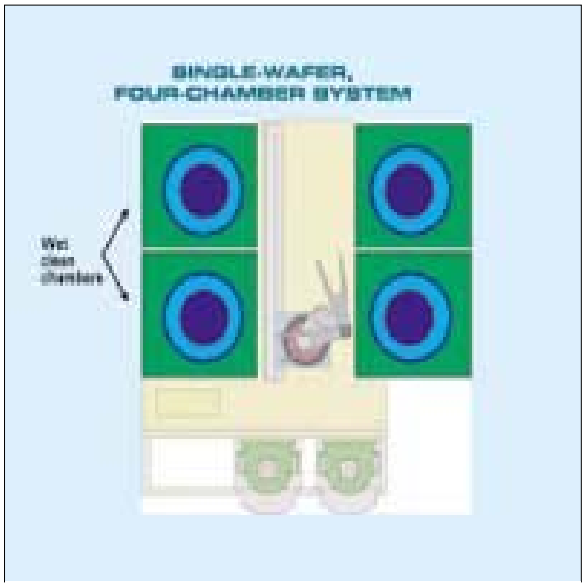
Production cycle time directly impacts a chipmaker's profitability. Since time-to-market is often critical, a single-wafer processing line enables more flexibility in lot scheduling and results in a faster cycle time and reduced work-in-process. Single-wafer processing also enables rapid prototyping and quicker development of new products.

Reducing the cycle time of the wet cleaning/etching step has a big impact on overall fab cycle time. In this paper, we will use the HF-SC1-SC2 dry cycle as a case study, but the results apply to most wet cleaning steps, which contain the RCA cycle or part thereof in some permutation. This step by itself is usually repeated up to 20× in some VLSI process flows. The same applies to other similar wet cleaning steps such as SPM-SC1-SC2 dry. Here we present a new process technology for wet cleaning that reduces the cycle time of a 1 hr process (DHF-SC1-SC2) to ~2 min. This implies that four wafers (or fewer) for this process can be completed in <2 min instead of >1 hr, and a full 25-wafer lot can take <15 min. In fabwide simulations, it has been shown that single-wafer processing applications can result in a >35% reduction in cycle time.

Chemical and hardware concept

In designing our new approach, we decided to build upon the conventional RCA chemistry (Fig. 2). To reduce cycle time, we shortened the dilute HF (DHF) etch from 5 min to <30 sec using a horizontal spin and dispense/spray concept that allows very short etch times with very good uniformity. High-concentration HF with very brief exposure times can be used in this approach; uniformities <1% (1σ) are achievable in a horizontal spin system, even with 15-20 sec etch times.

The traditional SC1-SC2 cycle, where each step takes ~10 min, can be reduced into a single step of 30 sec by using the following approach: The metal removal function of the SC2 can be combined into the SC1 by using a modified SC1 that includes chelating agents. The chelating agents take over the traditional metallic impurity



3. Drawing of a four-chamber single-wafer, short cycle time wet clean system.

removal function of the HCl, but work at high pH. Chelating agents in SC1 have been used before, such as the use of ethylenediaminetetraacetic acid (EDTA) in SC1 about 11 years ago.[6]

The SC1 process itself can be reduced from 10 min to 30 sec by using a much more efficient and novel full-coverage megasonics unit. In a conventional wet bench, the megasonics crystals typically are mounted on the bottom of the tank, and their energy is dispersed over 50-100 wafers. In a single-wafer horizontal spin solution, if the megasonics system is properly designed, the acoustic energy can be focused uniformly over a wafer, making it 50-100× more efficient.

The rinse time can be reduced from 8 min to 20 sec by using the same concept and centrifugal forces to reduce the boundary layer. In immersion wet benches, boundary layers on the order of 150 μm lead to long rinsing.[7] In a horizontal spin system, the boundary layers are much thinner (on the order of 10 μm), resulting in shortened rinse times.

The new cleaning approach incorporates a gentle, full-coverage, non-damaging megasonics unit that cleans more effectively and rapidly than existing technologies. Surfactants added to the SC1 avoid any redeposition of particles and help achieve a total process time of 30 sec. Drying relies mainly on centrifugal force (spin) to dry a wafer in 20 sec.

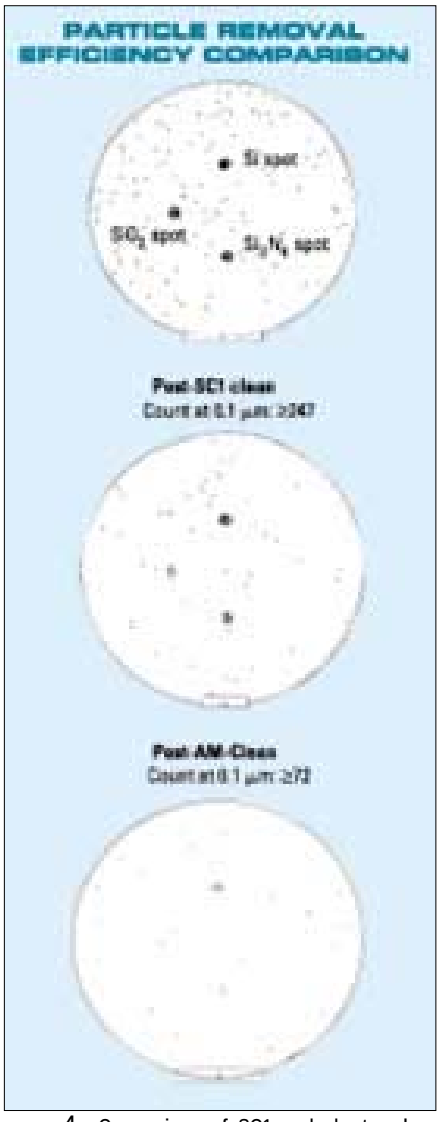
If we combine four horizontal spin chambers into a single system (Fig. 3), each chamber has a cycle time of 2 min for an HF-modified SC1 clean-dry cycle. Thus, a four-wafer lot can be processed in about 2 min. Such a system demonstrates a throughput of >100 wph, making it suitable for volume manufacturing.

Particle removal efficiency

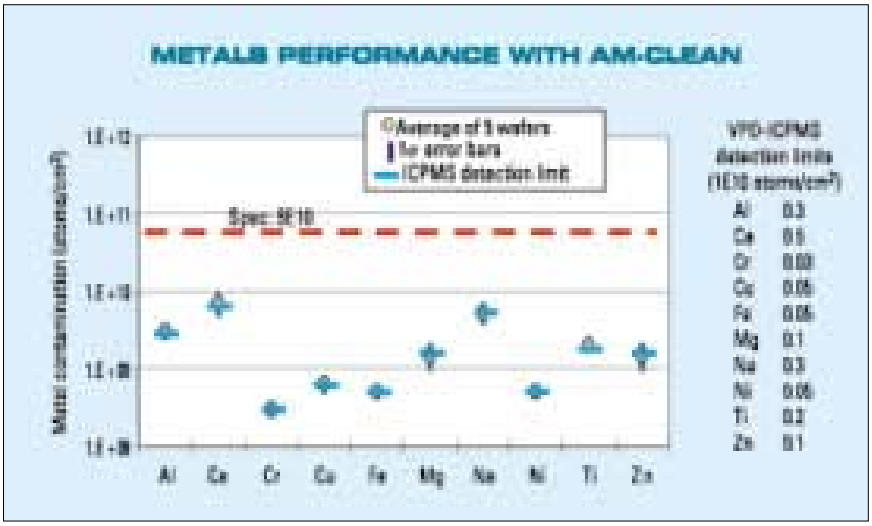
The addition of a surfactant to the SC1 solution greatly improves the particle removal ability of the SC1 chemical step. Surfactants increase a cleaning solution's effectiveness by helping it wet the wafer surface and dispersing (or carrying) particles from the wafer surface, all at very low concentrations. In addition, surfactants help suppress redeposition of very fine particles that are removed from the wafer surface (generally <0.14 μm) and ensure that fine particles stay in solution and can be easily rinsed later.

We investigated several types of surfactants and their ability to enhance the particle removal capability of our clean, concentrating mainly on anionic and non-ionic surfactants. A non-ionic surfactant that rinses from the wafer surface easily, leaves no residue, adds no organic or metallic contamination to the wafer surface, and is low foaming was selected. The surfactant also offers enhanced particle removal rates over a typical SC1, needs a low concentration to obtain critical micelle concentration (CMC) point and provides a high zeta potential.

We compared the Si_3N_4, Si and SiO_2 particle removal efficiency of the traditional SC1 and our short- cycle clean in a single-wafer cleaner with novel megasonics for a 30 sec clean on 300 mm wafers. The results are shown in Figure 4 . It is clear that the traditional SC1 does quite well on SiO_2 particles but has difficulty removing silicon particles. The surfactant added to the clean solves this deficiency. The SC1 clean removes only 90% of the silicon particles in 30 sec, whereas the modified SC1 clean (with surfactant) can remove up to 98% of these particles in 30 sec.



4. Comparison of SC1 and short-cycle AM-Clean for SiO2, Si and Si3N4 particle removal efficiency.



5. Metallic impurity levels after the AM-Clean are at or below the VPD-ICPMS detection limits.

Though Si_3N_4 particles are easier to remove than Si particles, Si_3N_4 particles are commonly used as the standard test for particle removal efficiency. For Si_3N_4 particles, the standard SC1 delivers a removal efficiency of 95%, while the modified SC1 clean (with surfactant) achieves 99% removal efficiency in 30 sec.

Metallic impurities

In aqueous solutions such as SC1, a silicon wafer surface is hydroxide terminated. The interaction of the metal ions in solution and the silanol surface groups can be described by the following equation where M^{x+} is the metallic ion:

$$\text{-Si-O-H} + M^{x+} \leftrightarrow \text{-Si-O-}M^{(x-1)+} + H^+$$

This equation is similar to the interaction of metal ions in solution with a weak acid ion exchange resin. We can see here that there are two ways to reduce metallic ions from depositing on the wafer surface.

The first is to increase the concentration of H^+. This is done by the traditional SC2 solution. Acidifying the solution at the same time produces a solution in which most common metallic ions are soluble, provided that a suitable oxidizer, such as dissolved O_2, H_2O_2 or O_3, is present in the solution to prevent any reduction, especially of such metallic ions as Cu^{2+}. However, this chemisorption/desorption equilibrium equation provides us with another mechanism for metallic impurity removal. If this is achieved by binding the free metal with a ligand so the combined complex remains soluble, we have created the same conditions for metallic impurity removal as the common SC2 solution. These ligands are often referred to as chelating, complexing or sequestering agents, one of the most popular being EDTA.

The advantage of this approach to metallic impurity removal is that the acid environment is no longer necessary. Metallic impurities can be removed from oxide surfaces at alkaline pH values using chelating agents, which are commonly used to remove particles such as the ubiquitous SC1 solution. This opens the door for an all-in-one universal cleaning solution, which is necessary to reduce cycle time when using single-wafer processing.

In our solution, we have used a chelating agent with a reduction in free ions of roughly 10^{35} for iron. We measured the metallic impurities after this clean to validate the combination of SC1-SC2 into a single step. The metallic impurities after this clean (Fig. 5) are below the VPD-ICPMS detection limit, which is on the order of 1E8 - 1E9 atoms/cm^2.

Organic residues

As mentioned above, we selected chelating agents and surfactants that can be completely rinsed. First, we measured the characteristic peaks in a time-of-flight secondary ion mass spectrometry (TOFSIMS) spectrum of the chelating agent and the surfactant by depositing a concentrated solution on the wafer and drying it in a nitrogen environment. TOFSIMS measurement following a clean and rinse cycle did not exhibit either the chelating agent or surfactant characteristic peaks. Hence, even a short 20 sec rinse effectively removes all traces of chelating agent or surfactant. This has been further evidenced by the absence of any particles on wafer surfaces that might indicate surfactant residues.

Process validation

Once the basic performance characteristics were established, a 10-day, >5000 wafer marathon with the DHF-AM-Clean process was carried out to validate this concept in a production environment. Wafers were sampled periodically to monitor all the basic characteristics of this clean such as throughput, reliability, metallic contamination, organic contamination, water consumption, chemical consumption, particle adders on the front and backside, particle removal efficiency, oxide etch uniformity and repeatability. The two biggest challenges in terms of repeatability for any cleaning process are the excursions of particles and control of the etch rate, especially wafer to wafer.

The particle removal efficiency of the modified SC1 clean with megasonics exhibits virtually 100% particle removal from both the front and backside of the wafer. During this marathon we measured all particles >0.12 μm. The starting particle count was generally <50 for particles larger than 0.12 μm. The area counts are included in the particle counts. Almost 99% of the monitor wafers exhibited <15 particle adders with an average value of <2 adders during the entire run. The tight control over particle excursion during an extended period of use indicates the stability of single-wafer processing and its ability to meet production requirements for stringent cleans.

Summary

In this paper, we have presented feasibility data for a new short-cycle wet clean (AM-Clean) using a single-wafer processing approach that offers excellent particle performance, oxide etch uniformity and metallic impurity performance. This clean combines the traditional SC1 and SC2 steps into one step by using the SC1 as the base and adding a chelating agent and surfactant to it. This allows the SC1 step to remove metals and particles in ~30 sec, when combined with an efficient megasonics set-up. Such short process times on a single-wafer platform enable high-throughput, fast-cycle-time processing that cannot be realized in batch systems. This clean meets or exceeds all regular performance metrics used to characterize cleaning, and has been proven production-worthy over an extended run.

References

1. W.A. Kern and D.A. Puotinen, "Cleaning Solutions Based on Hydrogen Peroxide for Use in Silicon Semiconductor Technology," *RCA Review*, 1970, Vol. 31, p. 187.
2. S. Verhaverbeke, et al, "Advanced Wet Cleaning Technology for Highly Reliable Thin Oxides," *Proc. of the Fourth International Symposium on Ultra Large Scale Integration Science and Technology*, 1993, Vol. 93, No. 13, p. 199.
3. T. Ohmi, "Proposal of Advanced Wet Cleaning of Silicon Surface," *Cleaning Technology in Semiconductor Device Manufacturing* IV, 1996, Vol. 95, No. 20, p. 1.
4. F. Tardif, et al, "Diluted Dynamic Clean: DDC," *Proc. of the International Symposium on Ultra Clean Processing of Silicon Surfaces, UCPSS* 96, p. 175.
5. D. Levy, et al, SEMATECH Cleaning Workshop, Austin, Texas, May 21-22, 2002.
6. S. Verhaverbeke, et al, "The Effect of Metallic Impurities on the Dielectric Breakdown of Oxides and Some New Ways of Avoiding Them," *Tech. Dig. IEDM*, 1991, p. 71.
7. L.M. Loewenstein and P.W. Mertens, "The Rinsing Problem: Effect of Solute-Surface Interactions on Wafer Purity," *Solid State Phenomena*, 1999, Vol. 65-66, p.1.

Steven Verhaverbeke is technology manager for Applied Materials ' Wet Clean Division (Materials Transistor and Capacitor Group), focusing on development of new wet cleaning concepts and processes. He received his Ph.D. in applied sciences from Katholieke University.

Satheesh Kuppurao is marketing manager and strategic technologist for Applied's Wet Clean Division. He has a Ph.D. in materials science from the University of Minnesota and B. Tech from the Indian Institute of Technology.

Christopher Beaudry is a member of the technical staff for Applied's Wet Clean Division. He received a Ph.D. in ceramic science and engineering from Rutgers University.

J. Kelly Truman is general manager of Applied's Wet Clean Division. He received a B.S. in metallurgical engineering and materials science from the University of Notre Dame, and M.S. and Ph.D. degrees in materials science and engineering from the University of Florida.

Wafer Cleaning Processes – A Review

Sreenivas Jayaraman

ECE 384, University of Illinois, 1406 West Green Street, Urbana, IL 61801

Abstract

Increasing miniaturization of devices along with high yield and reliability requirements has made the process of wafer cleaning a very critical step in IC production. This paper reviews the sources of contamination and objectives behind a cleaning operation. The conventional RCA clean has its shortcomings due to the strong acids and bases involved, accompanying health and environmental issues and high cost. Novel cleaning processes like ozonated DI water treatment, IMEC clean, UCT process and others offer several advantages over the RCA clean. They are made of fewer process steps and have greatly reduced chemical consumption. Not only are they *greener* they also cost much less to operate. Such processes are the stages in the march towards the final destination in the cleaning roadmap – a single wafer, single step clean.

1. Introduction

Semiconductor industry driven by the need to produce faster and cheaper computers is seeing increasing miniaturization of integrated circuits. Nanometer scale devices coupled with stringent reliability requirements has only made wafer cleanness a very critical parameter in processing. It directly affects the Gate Oxide Integrity (GOI), which in turn is closely related to the lifetime of the device. With gate oxide thickness of 25-70Å and gate length of the order of 0.35-0.1 μm (1) any residual or organic contaminant can kill the device. Wafer cleaning is especially critical before any diffusion, anneal, CVD or oxidation step. The number of cleaning steps that wafers have been undergoing has risen steadily over the years as illustrated in Fig. 1.

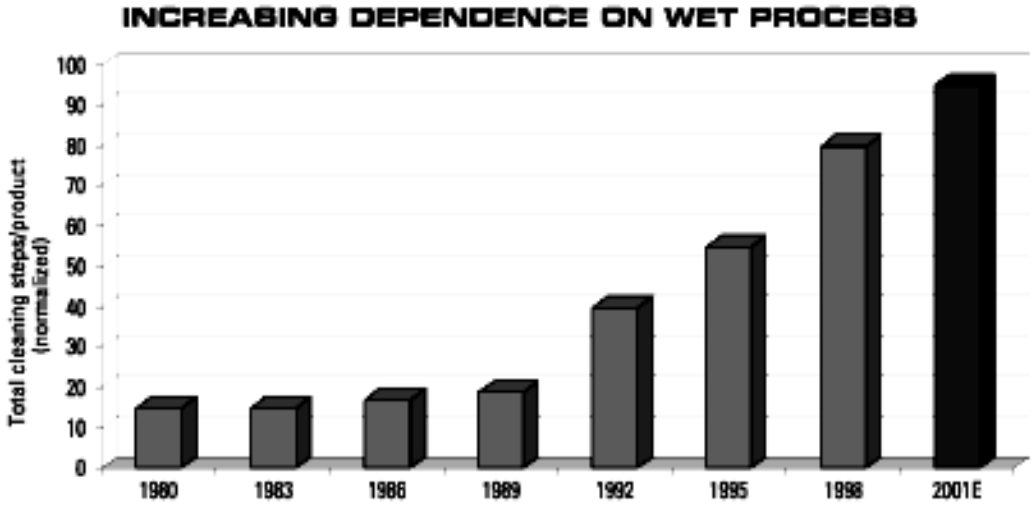


Fig. 1: ***Stronger demands to keep contamination under control, as well as an increasing number of metal layers, contribute to a rise in the number of wafer cleaning steps in the manufacturing process. (Source: VLSI Research) (ref. 7)***

The RCA clean (2) with minor modifications still forms the backbone of major front-end wet cleans. The chemicals involved (H_2SO_4, HF, NH_4OH) are costly to store, difficult to handle and need a full-fledged infrastructure to dispose. The environmental and health issues associated with the exposure to strong acids and bases involved cannot

be overemphasized. Alternatives to the RCA clean that are both low cost and environment friendly are hence in focus. The following paper describes the basic objectives behind any cleaning procedure, the existing conventional technique and emerging processes that may replace it.

2. Objective of wafer cleaning

Before the wafer is processed upon or between processing operations (diffusion, oxidation etc.) it undergoes several cleaning procedures to take care of contaminants on its surface. These include (3) –

a) Dirt and Dust – It is a natural consequence of the exposure to the environment. The source may be a pre-processing step like dicing, sawing, storage boxes, human contact or the atmosphere of the 'clean' room.
b) Native oxide – It is formed when Si is exposed to air or may be remnant from some previous processing step and is usually thin (<100Å). This oxide may need to be stripped and any residual oxide may act as a barrier to any chemical treatment that the wafer has to undergo
c) Organics – Organic contamination is from human contact, prior processing step like photolithography or wafer storage boxes that are usually made of polymers.
d) Metallic residues – A major source of these are acids and organic solvents that are being used to treat the wafer or manual handling by tweezers. Hence, the need for 'electronic grade' solvents cannot be overemphasized.

The contaminants can affect the device reliability as follows –

- Decrease in oxidation rate and oxide quality
- Low breakdown field and high leakage current caused mainly by metallic contaminants
- Introduction of metal impurities from the surface into silicon during diffusion, CVD and other high temperature operations may lead to formation of carrier trap and recombination centers, hence reducing minority carrier lifetimes. It may also lead to threshold voltage shift and hot carrier degradation.

The presence and level of contamination is characterized both by simple methods like visual observation and advanced techniques. The common method to check for etch completion in oxide etching is to see the wetting of water on Si surface; water does not cling to a silicon surface free of oxide. Particulate contaminants can be observed by a surface scan under a high power microscope with a profilometer. For very fine particulate matter an Atomic Force Microscope (AFM) can be used, which yields surface roughness and particulate data in the nanometer range. Organic contamination and, especially, metallic contamination calls for advanced techniques like Secondary Ion Mass Spectrometry (SIMS) and time-of-flight SIMS. Other techniques include vapor-phase decomposition, and X-ray fluorescence. In light of the above discussion, it is clear as to why wafer cleaning is a very important step in any electronic fabrication.

3. RCA Cleaning Procedure

RCA standard clean was originally developed at the RCA solid-state division in New Jersey in 1961 (2). The process involves treating an already degreased wafer in two solutions SC-1 and SC-2. SC-1 is made up of 4:1:1 to 6:1:1 of H_2O, 30 w/w% H_2O_2 and 29 w/w% of NH_4OH. This solution at elevated temperature removes residual organic contaminants by oxidative breakdown and dissolution. It also removes noble metals like Ag, Au, and Cu through complex formation with NH_4OH. SC-2 is made up of 4:1:1 to 6:1:1 of H_2O, 30 w/w% H_2O_2 and 37 w/w% of HCl. Used at 75 to 85 ^oC, this low pH solution effectively removes alkali ions and any other remaining metal impurities. Dissolved ions form soluble complexes and are hence prevented from re-depositing on the wafer surface. An oxide etch is done in HF before going from SC-1 to SC-2. There have been minor modifications suggested to the process like H_2SO_4 in place of HCl in SC-2. Also, there have been some process technology changes like the use of centrifugal spray cleaning and megasonic cleaning. In the former, an automated system sprays a fine mist of reagents and water on the wafer surface ensuring a fresh supply of reactants on the wafer surface, efficient removal of by-products and reduced volume of chemicals needed. In megasonic cleaning ultra high frequency sound waves provide scrubbing action on wafers immersed in the cleaning solution. In spite of its efficacy, the RCA process has major drawbacks, the chief among them being the strong acid and bases involved, as mentioned before. SC-1 and SC-2 need separate fume hoods as NH_3 and HCl form dangerous smog of NH_4Cl. Fused silica containers for the solutions and high grade polypropylene containers for wafers are some other stringent requirements.

4. Novel Cleaning Procedures

Most novel cleaning techniques that have been developed are driven by the need to reduce the consumption of chemicals and ultra pure water (referred as UPW, DI water etc). This brings down the process cost and also makes the process 'greener'. This section describes a few such techniques and the concomitant advantages.

4.1 Ozonated DI water (DI/O_3)

Ozonated DI water has been extensively studied (4,5,6) to replace strong chemicals like sulfuric acid, hydrogen peroxide and ammonium hydroxide from front-end critical cleans. DI/O_3 solution is prepared by dissolving large amounts of ozone in DI water under pressures of 2-3 bar. The critical concentration of ozone needed for efficient cleaning is 60-120 ppm. A centrifugal spray system dispenses the solution on the wafer and since contact time involved is short very little ozone is lost from the solution. The typical cleaning sequence involved is DI/O_3 – HF– DI/O_3, with HCl added to any or all of the steps depending on the need to remove metallic impurities. The DI/O_3 is a very effective oxidizer and wafer readily forms a chemical oxide on exposure. Most of the particulate contaminants are trapped in the oxide and are removed in the subsequent etching step with HF. Olson et al. (5) have reported the particle removal performance and surface roughness on Si surface post treatment with DI/O_3 processes (Fig. 2). DI/O_3 – HF– DI/O_3 sequence showed a negligible change in surface roughness and 92% particle removal efficiency.

DI/O_3 process offers a huge environmental advantage in terms of water and chemical usage. The water usage is cut by almost 50% and chemical usage is either drastically reduced or eliminated. These are also the conclusions arrived at by Olson et al. (5) in comparing this clean with a standard B –clean. The latter is a sequence of four steps – SPM (H_2SO_4, $H2O_2$), HF, SC-1 and SC-2. It is also offers as process time reductions as we cut down upon several rinsing and pre-rinsing operations.

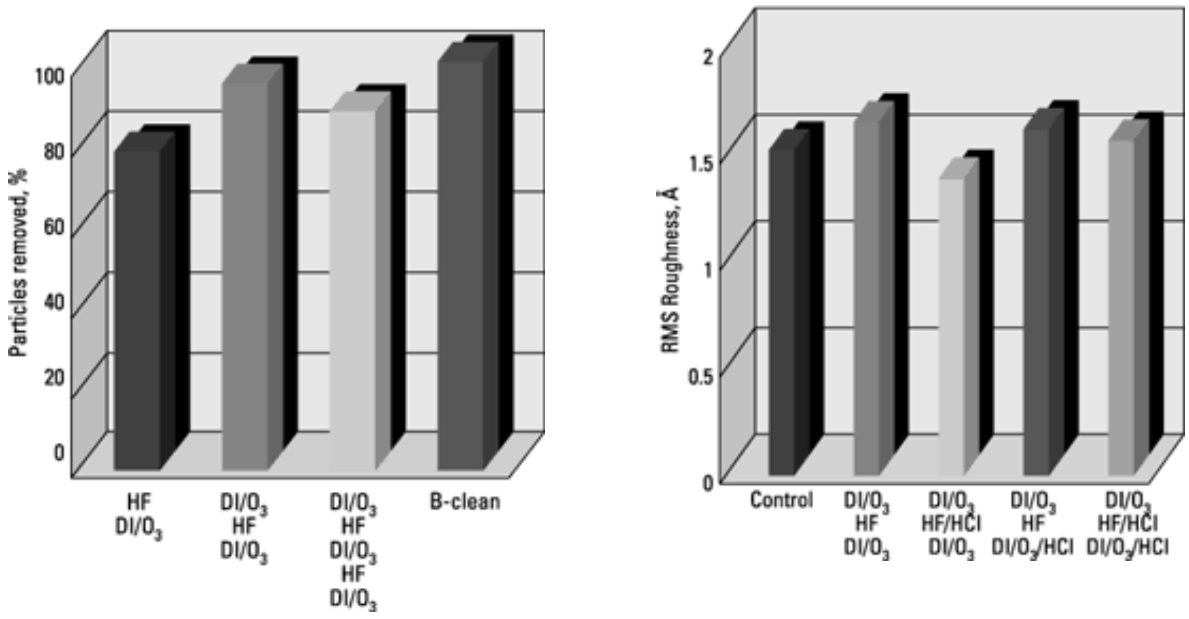


Fig. 2: Particle removal efficiency and surface roughness after different DI/O_3 – HF– DI/O_3 treatments and B-clean (ref. 5)

4.2 IMEC-Clean As the name suggests, it is a process developed by the research labs of IMEC – Belgium (8). IMEC-clean involves a two-step approach; in the first, a strong oxidant is used to remove organics from the surface. The wafers are treated with a sulfuric acid/ozone mixture (SOM) at 90 ^{o}C followed by hot and cold DI water rinse. The wafer is left with a uniform oxide on its surface after this step. The second step is the stripping of oxide in dilute HF; 0.5 molar HCl is added to HF to dissolve any metal impurities as needed. As the oxide etches it lifts off any residual particles. Subsequently, rinsing is done in ozonated DI water (DI/O_3) in a megasonic bath. The water is kept at pH =2 by adding HCl and are then marangoni dried at pH=3. This process summarized in Fig. 3, leaves the wafer surface hydrophilic as there is a very thin layer of chemical oxide. Adding HCl

during rinse and dry keeps the pH below the isoelectric point of silicon oxide. This ensures particle removal and

	Metal concentration on the wafer (10^{10} atoms/cm2)			
Contaminant	**Ca**	**Fe**	**Cu**	**Zn**
Initial concentration	154.4	5.6	4.4	1.8
Modified RCA clean	<0.26	0.2	0.4	0.2
IMEC clean	<0.26	0.1	<0.07	0.08

Table 1: Metal removal efficiency for a RCA clean vs IMEC clean in the same wet bench (ref. 9)

prevents re-deposition due to repulsive zeta potentials (8). Table 1 and Table 2 present data to support the efficacy of IMEC-clean. IMEC appears to do better than RCA in metal removing efficiency and is almost 100% efficient in removing usual particulate contaminants. Measurements of defect densities, in capacitor structures fabricated on oxidized wafers cleaned by IMEC and RCA clean, yielded values below or close to the detection limit of 0.1 defect/cm^2. Table 3 presents the cost of ownership comparison between IMEC and RCA process. The important figure here is volume of chemical waste generated by the RCA process and the huge advantage offered by the novel processes in this regard.

Particle Type			
Substrate	**SiO_2**	**Si_3N_4**	**Al_2O_3**
Si	0.99	1	1
TEOS	1	0.99	1
SiO_2	1	1	1
Si_3N_4	0.94	0.98	1

Table 2: Particle removal efficiency for an IMEC clean on different substrates (ref. 8)

4.3 UCT-Process

The Ultra Clean Technology (UCT) process is based on impurity adsorption and removal from the silicon surface. This process also relies on ozonated-ultra pure water (UPW) for the cleaning action. When first introduced (4) the process sequence was DI/O_3 – HF– DI/O_3, the efficacy of which has already been discussed. The second step

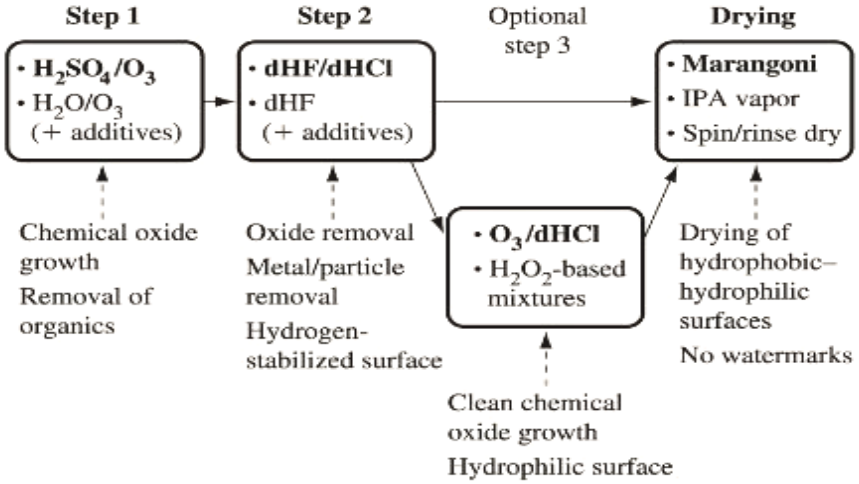


Fig. 3: Schematic illustration of IMEC-Clean (ref. 9)

	Conv. RCA	IMEC	%
Chemical Baths	4	2	50
Rinse Baths	5	2	60
DI-water/yr	$26x10^6$l	$8.7x10^6$l	76
Chem. Waste/yr	$336x10^3$l	$20.8x10^3$l	94
IPA/yr	$17.5x10^3$l	$0.4x10^3$l	98
Exhaust/yr	$60.5x10^6$l	$22x10^6$l	64
Bench length	8m	4m	50

Table 3: Cost of ownership comparison for a conventional RCA clean (SPM/SC-1/DHF/SC-2/IPA vapor dry) and IMEC clean (ref. 8)

in the sequence also had some H_2O_2, some surfactant and a megasonic treatment. The UCT process in the current state (6) with the purpose of each step has been delineated in the flow chart in Fig. 4. As illustrated, the process utilizes very little quantities of any strong chemicals and is made of four steps in all. It is also easy to reclaim the water used and recycle it

after proper treatment. This process hence offers great promise in terms of cost reduction and environmental safety and health (ESH).

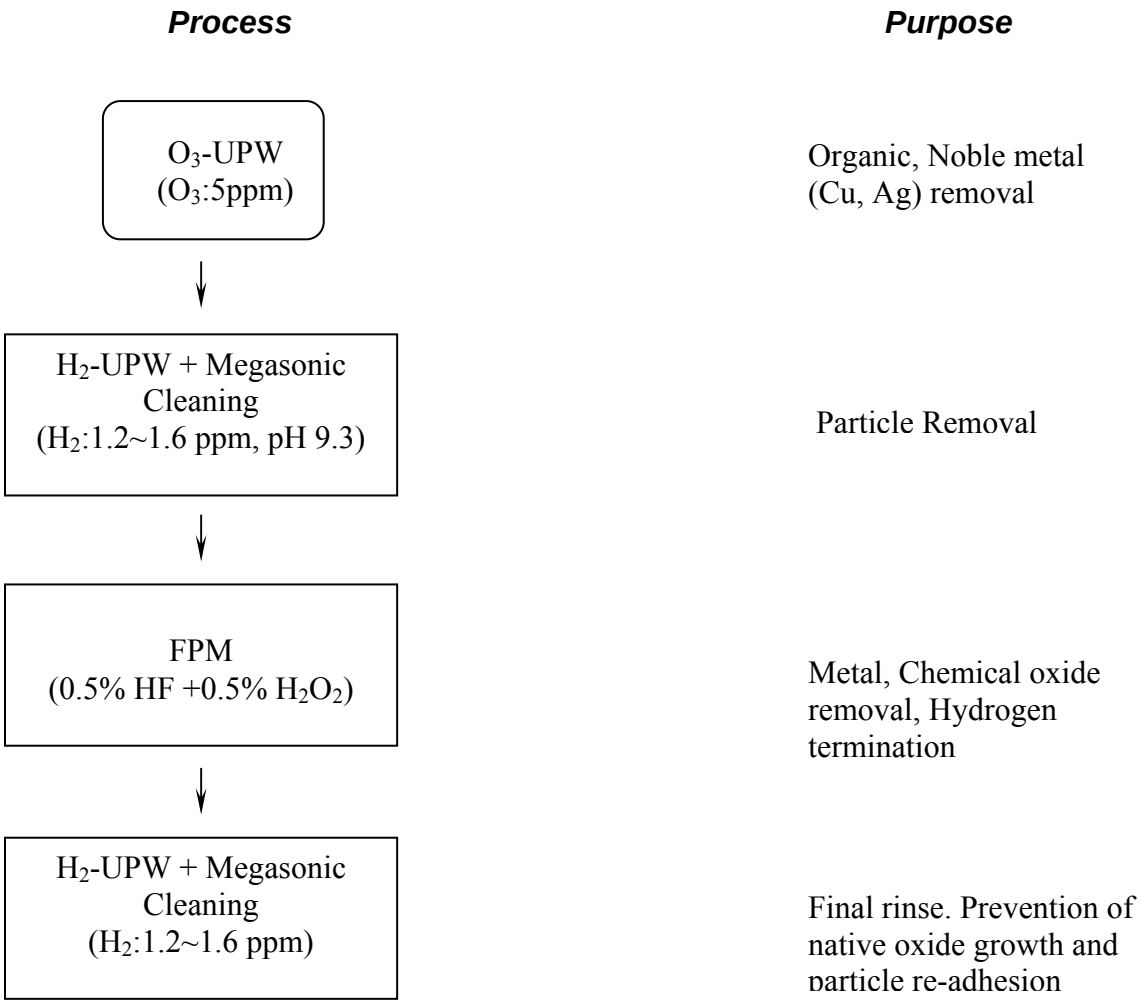


Fig. 4: Process flow in UCT process

4.4 Other Cleaning Processes

A one-step method suggested by Pan et al. (10) involves putting some additives in the conventional SC-1 solution. These include tetra-methyl ammonium hydroxide (TMAH), a surfactant and ethylenediamine tetra-acetic acid (EDTA), a chelating agent. TMAH helps in removing particles while EDTA reduces metallic contamination. Their optimum recipe was made of TMAH in NH_4OH in the ratio of 1:50, 100 ppm of EDTA and operating temperature of 60^{o}C. MOS capacitors made from wafers cleaned using this process showed an improvement of at least 50% in leakage current value and 1-1.5% improvement in electric breakdown field compared to those subjected to conventional clean.

Aqueous foam is another novel technology under active research as a cleaning solution (11). The collapsing aqueous foam bubbles provide the cleaning action here, a process similar though more efficient than the megasonic bath. Since a major part of foam is made of gas phase the total volume actual aqueous reactants is very less. The cleaning action is not compromised even though reactant and solvent consumption is far reduced.

A major source of contamination on the wafer is the solvents themselves that are being used to clean them. Hence, one way of obtaining ultra-clean wafers is to resort to a totally dry-clean. One such process uses the photochemical UV/Cl_2 technology (12) to prepare the surface for critical operations like epilayer deposition, gate oxidation etc. An oxide layer is grown in a rapid thermal oxidation chamber and anhydrous HF is used to etch the oxide. Chlorine gas is then flown over the wafer surface in a dry vacuum chamber, with UV lamps on either side of the wafer. Chlorine disassociates activating the surface reactions that removes organics and trace metal contaminants. Careful control is

needed to avoid the wafer surface from roughening during this process. This process was initially designed as a final clean after some sequence of wet cleans to remove bulk contaminants. This clean process has led to improved performance of devices with ultra-thin (10 Å) gate oxides.

4.5 Conclusion

Wafer cleaning operation was reviewed in light of ever increasing reliability requirements and shrinking device scale. The research in this area is being driven by the need to obtain better results with fewer operational steps and reduced chemical consumption. O3/HF/O3, IMEC clean and UCT clean are some new techniques that score over

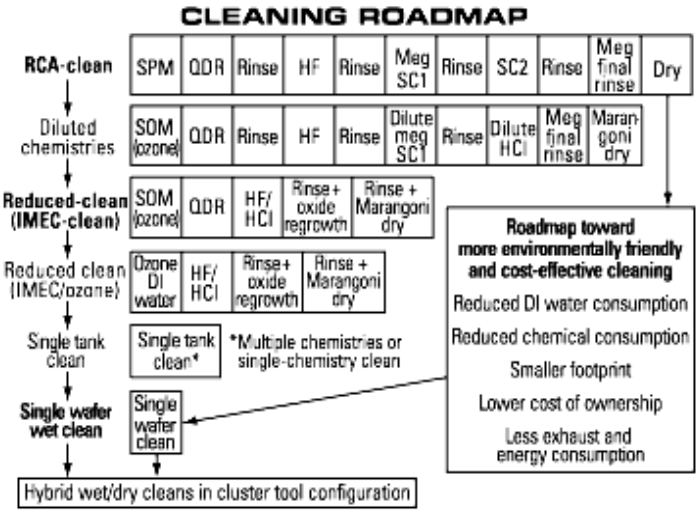


Fig. 5: Progressive steps to a single wafer wet clean (ref. 13)

RCA clean in chemical consumption, environmental and health safety, cycle time and hence reduced cost. They are equally efficient and at times even better than the RCA process. The future as illustrated in the roadmap in fig. 5 could be cleaning the wafers individually in one step with multiple chemistries operating at the same time.

References

1. Semiconductor Industry Association: The National Roadmap for Semiconductors (SIA, 1997)
2. W. Kern and D. Poutinen, RCA Rev. 31, 187 (1970)
3. G.E. Anner, Planar Processing Primer (Van Nostrand Reinhold, New York, 1990)
4. T.Ohmi, J. Electrochemical Society 143, 2957 (1996)
5. E.D. Olson, C.A. Reaux, W.C.Ma and J.W. Butterbaugh, Semiconductor International, Aug (2000)
6. H. Morita, J.Ida, T. Ii and T. Ohmi, IEEE International Symposium on Semiconductor Manufacturing Conf., 453(1999)
7. A. Hand, Semiconductor International, Aug (2001)
8. M. Meuris, S. Arnauts, I. Cornelissen, K. Kenis and M. Lux, IEEE International Symposium on Semiconductor Manufacturing Conf., 157(1999)
9. M. M Heyns et al., IBM J. Res. Develop. 43, 339(1999)
10. T.M. Pan, T.F. Lei, T.S. Chao, M.C. Liaw and C.P.Lu, Jpn. J. Appl. Phys 39, 5805 (2000)
11. M.A.Lester, Semiconductor International, Feb (2002)
12. M.A.Lester, Semiconductor International, Dec (2000)
13. M.A.Lester, Semiconductor International, Feb (2001)

Appendix D - Photoresist Processing

Photoresist Chemistry

The ECE 444 lab currently uses SHIPLEY 1813photoresist (PR) because it's safer than most and because it can be processed as either positive or negative PR. It is also the choice of many researchers. It is one of the cheapest photoresists on the market at ~$1000 per gallon. Luckily, the chemistries for all positive photoresists are similar so learning about this one will not be for naught. Photoresists all contain 3 basic components: an organic polymer (usually novolak resin) which is what "resists" etchants, a solvent carrier (usually an acetate) so it's a liquid for easy application by spinning, and a photoactive component often called a sensitizer (usually a diazoquinone), which causes the solubility to become dependent upon exposure to UV radiation.

SHIPLEY 1813uses novolak polymer, propylene glycol monomethyl ether acetate (PGMEA) solvent, and diazonaphthoquinone as the sensitizer. On the next page is the chemical reaction used to create the novolak resin. Below that are the three distinguishable reactions undergone by the sensitizer attached to the novolak matrix during exposure. Note that some water is actually required.

For image reversal (negative) processing the indenecarboxylic acid is decomposed by a post exposure bake giving off carbon monoxide and rendering the sensitizer insoluble to the alkali developer. The previously unexposed sensitizer can then be made soluble by a subsequent flood exposure. Since there is no longer sensitizer in the previously exposed areas they will remain insoluble.

Most of the instructions for patterning with photoresist are included in this appendix, but the operation of the Ultratech steppers is described in Appendix H. Some specific variables, such as etch time, which mask to use and whether to use the image reversal technique, are left to the experiment which references this appendix. The tasks presented here take place in three locations and, therefore, are split accordingly into directions suitable for posting at the spinner hood, the development station, and the PR removal station.

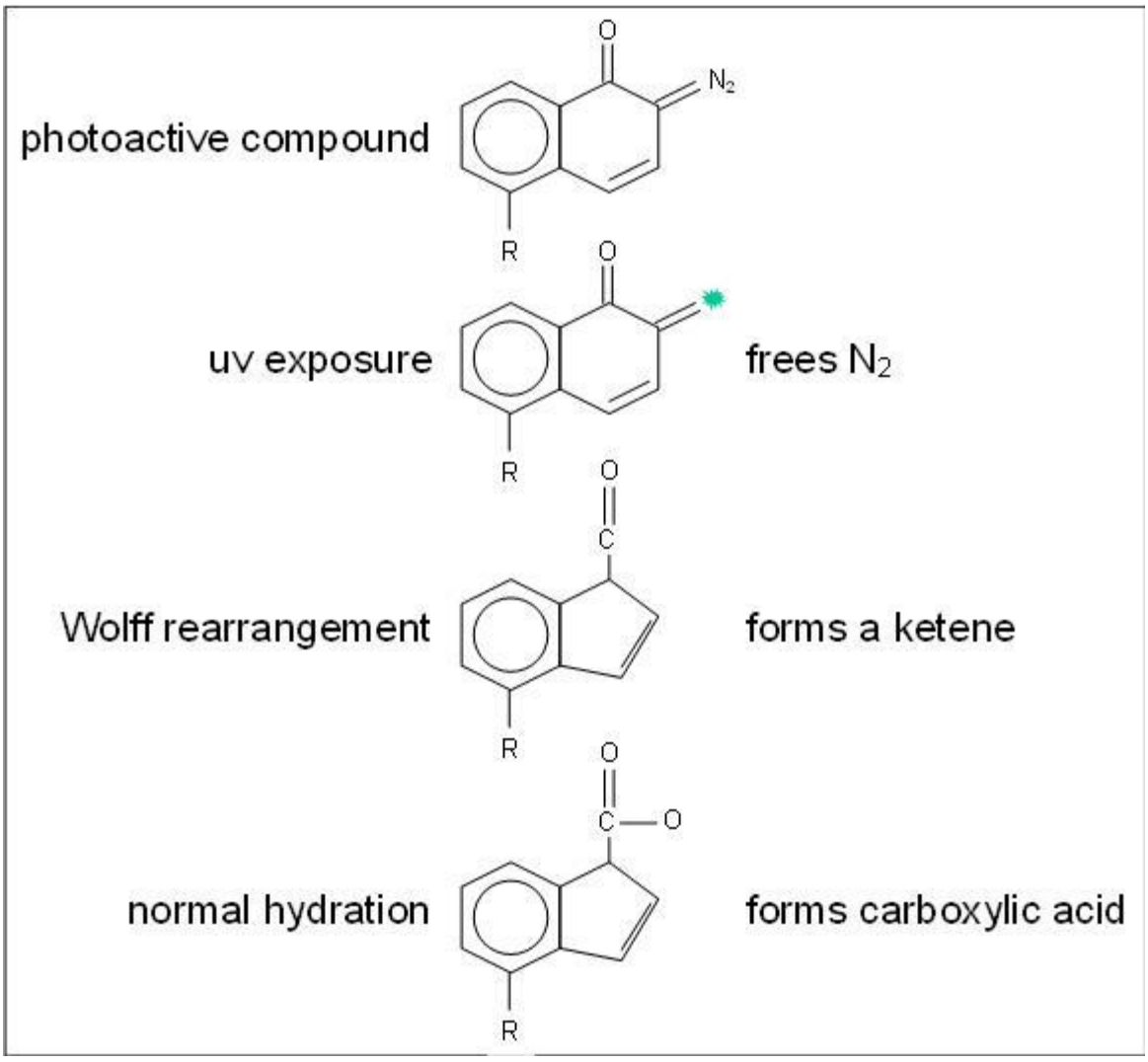


Figure: Exposure sequence for positive tone photoresist.

Preparation of Photoresist

Before beginning, record the conditions of the PR room and equipment by making entries in your logsheet. The wafer surface should be scrupulously clean before beginning this process.

Drive any moisture out of your wafer with a 2-minute dehydration bake on the bakeout hotplate (3 minutes if the room humidity is >60%). While you wait, check that the spinner is set for 30 second duration.

Allow your wafer to cool on the 'cool block' for 20 seconds. Wipe off the spinner chuck with a Kimwipe while waiting.

Center the wafer on the spinner chuck and start the spinner by momentarily pressing the front of the foot switch.

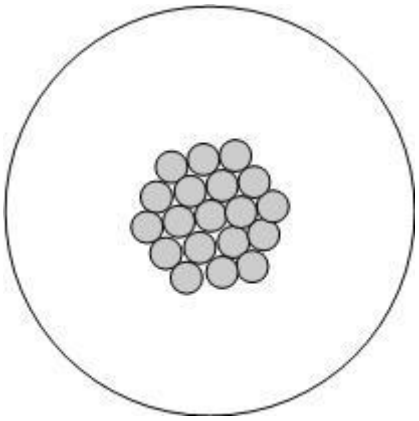
While the wafer is spinning, spray it with nitrogen from the N2 arm and check that it is indicating that it is spinning at 3000 rpm.

Vacuum is applied to the chuck only while spinning. You may stop the spinner by pressing the back of the foot switch, but don't continue blowing nitrogen on it when it stops. The spinner will automatically stop after the preset time.

While the spinner is spinning the wafer, drop 6 drops of hexamethyldisilazane (HMDS) onto the center of the wafer and stop the spinner as soon as the appearance of the wafer remains constant.

HMDS behaves as a surfactant, a wetting agent. It helps the photoresist adhere better. Think of it much like a detergent. In this case, the organic end (hexamethyl-) of the molecule is similar to and binds well to the organic PR. The silazane end, being silicon based, sticks well to the wafer/oxide surfaces (this is a simplistic description of the mechanism - see if you can find the actual mechanism in Grainger). It even seems to help adhesion on aluminum as well.

Immediately place 35 to 40 drops of SHIPLEY 1813positive resist on and around the center of the wafer using the filtered syringe. A pattern like that below works well for the first 9 drops. Use the last few to fill in any voids between the drops. Use extra drops if necessary to fill all interior dry spots within the PR puddle.



Wait at least 5 seconds after the drops completely flow together, then start the spinner. This time, let the spinner stop by itself.

Complete coverage of the wafer is critical to the operation of the steppers. There are targets on the wafer which must not be etched away. If your wafer is not completely covered, ask your TA since there are places which can be etched while still allowing the stepper to perform. Check the uniformity of the resist by looking for a bull's-eye effect - if you see it, it is not uniform (which is not critical to our process - what problem does nonuniformity cause?). The thickness of the PR is ~1.6µm, and exhibits thin film interference effects, much like oxide. The color of the film is altered by varying thickness.

Bake for 45 seconds on the Softbake hotplate.

Allow the wafer to cool for a few seconds on the 'cool' plate.

The photoresist is now ready for exposure to ultraviolet light through a mask. Refer to the instructions for the stepper (Appendix H).

If image reversal is desired, expose for a dose of 125mW cm2/sec. Follow the exposure by a 60 second bake on the reversal bake hotplate and a 20 second flood exposure. This may reduce the development time unless more dilute developer is used.

Develop until pattern is sharp (see the Development procedure to be posted on developer hood.)

Finally, complete the preparation of the PR for use as an etch stop by performing a 60 second hardbake on the hardbake hotplate (currently the same as the softbake hotplate).

Cool the PR for a few seconds on the 'cool' plate before putting it in the wafer carrier.

The photoresist is now ready for etching (or deposition if using the lift-off technique).

DEVELOPMENT

Dip development has the advantage of not pitting the surface of the PR and is used for development of the 4" wafers, although careful inspections must be followed since development slows as the PR loads up after multiple wafers have been processed. In industry, 500rpm spinners beneath a low velocity nozzle are common.

4" Immersion Development

1. It is strongly recommended that you change the D.I. rinses before beginning.
2. Open the faucet valve just barely enough to maintain a continuous stream (as opposed to a sequence of individual drops.)
3. Make sure there is sufficient developer in the developing container to cover the entire wafer. If not ask your TA to fill it.
4. Check the number of times that the developer has been used. If you are the first user, you will develop for ~40 seconds (do not use this as an exact time – this is just a guideline). Each additional wafer that is developed will probably take slightly longer (although this depends on the resist thickness).
5. Immerse the wafer into the developing container and begin timing.
6. Gently agitate the wafer and develop for the time determined from above.
7. Quickly quench the developer in the first DI rinse. Be careful not to break your wafer by swishing it too fast in the rinse.
8. Note the time.
9. Move to the FINAL RINSE tank for at least 10 seconds while you calculate the total time spent developing.
10. Gently rinse your wafer with DI from the faucet (near the nozzle) and N2 dry (NO IPA.) Excessive water velocity can pit the surface of the PR. Although this is not usually a problem, it does look bad until the PR is removed. Fresh DI from the sprayer is used in case the rinse tank has enough PR in it from previous students to

deposit a thin invisible film on the wafer. Students may change the DI rinse at their own discretion.

11. Return the wafer to the carrier face up.
12. Gloves and tweezers should be rinsed in D.I. if developer is suspected on them. Used developer is highly water soluble, but can be difficult to remove if left to dry on things.
13. Inspect the development under a UV filtered microscope. Pay particular attention to the smallest windows to be opened. They may take a little longer to develop because it's harder for fresh developer to reach the bottom to dissolve the PR. Gross under development will appear as splotches with multicolored rings in the larger areas which should be clear of PR. Why?
14. Repeat in 10-second intervals if necessary.

Discussion

The solubility change during exposure of photoresist is a couple of orders of magnitude at best (although chemists are constantly improving it). Consequently, all the PR will eventually dissolve in the developer. Before that happens the openings in the PR will widen and loose their sharpness. Therefore, development time should be minimized. The smallest windows which are to be opened are usually the limiting factor because fresh developer must diffuse down to the surface in order to do its job. This diffusion is slowed when the width of the window in the PR is comparable to its depth. A possible technique to minimize this effect would be to hold the wafer at an angle so the PR could not puddle. Unfortunately, PR adhesion and sprayer uniformity become greater problems (at least in ECE 444 lab). A compromise seems to be the best solution. Periodic tilting of the wafer to help change the developer in the small windows is suggested. Exactly how often is optimum has not been determined. Record any useful observations you make which would help in your notebook.

Photoresist Removal

After the etch, the PR may be removed by one of the following three methods. Do not try one of the other methods before performing the microscope inspection step.

Use acetone, PGMEA, or other solvent to remove the majority of the PR by making a puddle of the solvent on the wafer while holding it level above the proper waste container. Pour the solvent off after 10-15 seconds and repeat until there is no significant improvement. Finish with a standard degrease - squirt with acetone, IPA, water, IPA again, and N2 dry.

Use the plasma asher. See Lab→Equipment→Asher on the web page for instructions. This is the most reliable method, but also the most time consuming. Please try it at least once during the semester.

Use acetone, PGMEA, or other solvent to remove the majority of the PR as in the first method. Then use heated Posistrip, Microposit Remover, or other proprietary positive PR remover. DI rinse, N2 dry.

Inspect for Residual PR Under a Microscope

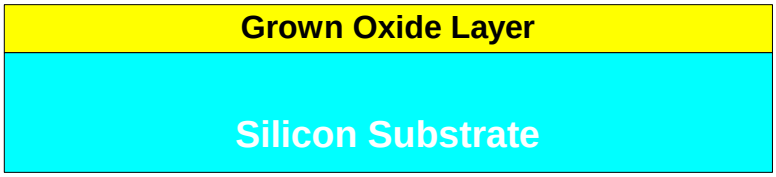
Pay particular attention to the rim of the wafer where edge beading during the spin on process left extra thick PR. Removing the yellow UV filter from the illuminator will help you see PR, but be sure to return it. The residue will often look similar to slightly underdeveloped PR. Since such residues are likely to be very thin with respect to visible light wavelengths, they often take on a rainbow of colorations as the thickness variations cause different interference patterns. PR is a furnace contaminant and must be completely removed. The whole class is counting on you keep the furnaces clean.

If PR residue is detected, go back to step 1. If there is only a little left, additional soaking with acetone will usually take care of it. Stubborn PR may need the plasma asher however. Occasionally, etched features will look like PR residue so consult with your instructor before going back to step 1 a third time.

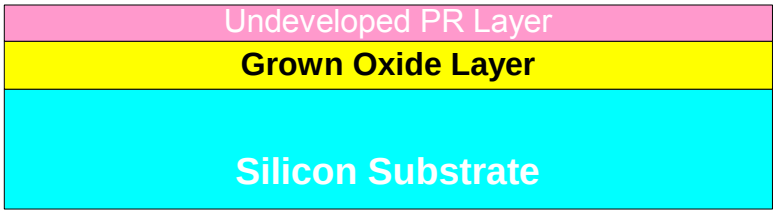
PR Process Overview

1. Start with bare silicon wafer.

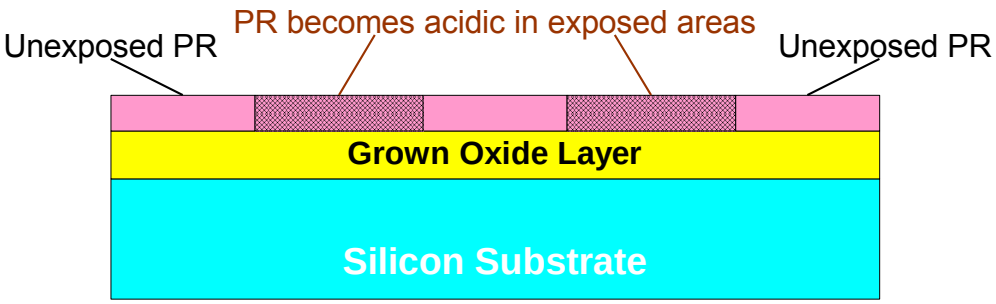
2. Grow oxide on wafer surface.



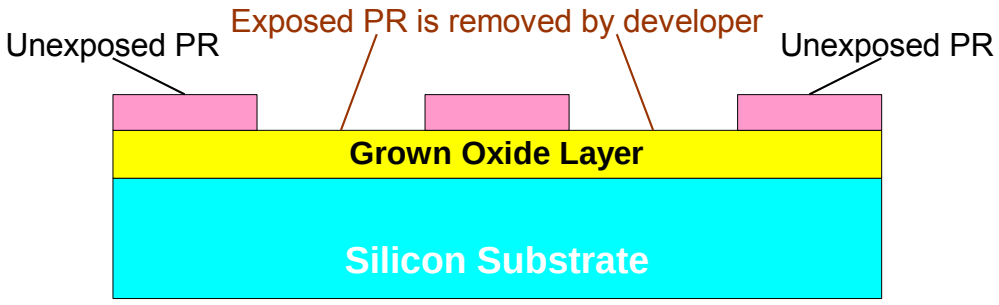
3. Apply PR.



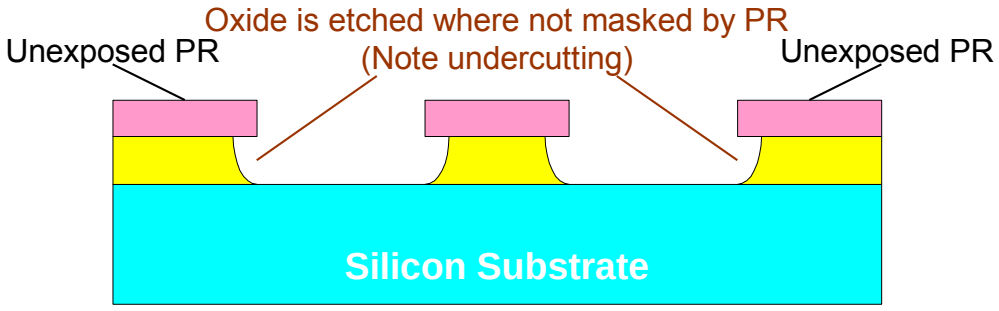
4. Expose PR. Positive resist becomes acidic in exposed regions.



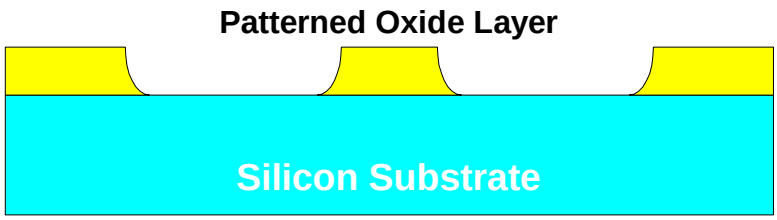
5. Develop PR. PR will act as etch stop.



6. Etch oxide. PR stops etch in undeveloped regions. Note undercutting due to isotropic nature of chemical oxide etch.



7. Remove PR. End result is patterned oxide layer on surface of wafer.

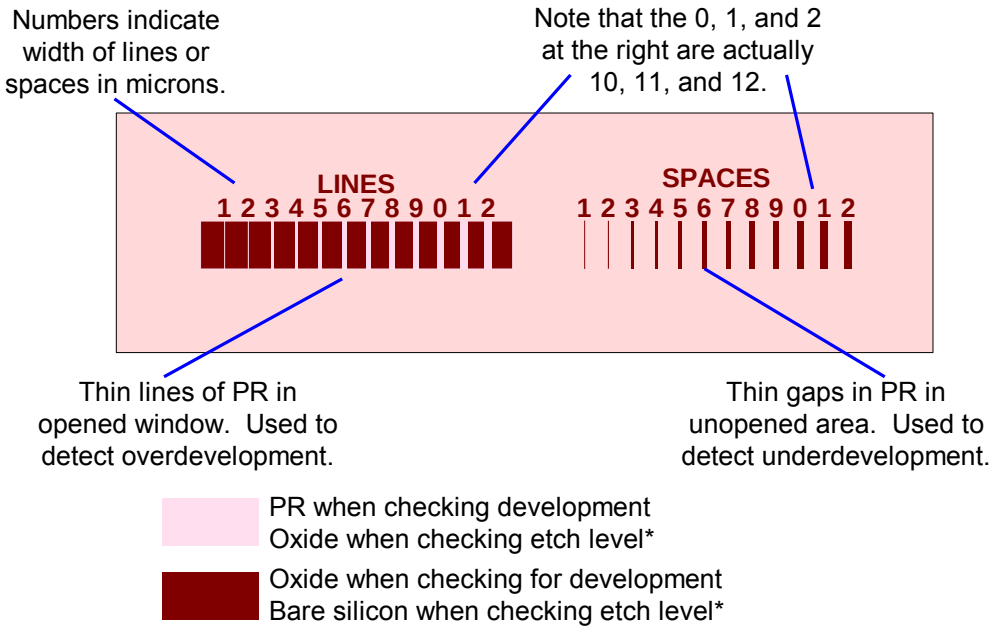


Wafer Inspection

At various points in the processing of your wafer, you will need to inspect it under the microscope. After PR removal, you will want to inspect your wafer carefully for any remaining PR residue. In general, you will be looking at the "Lines" and "Spaces" patterns to determine the level of development and the level of etch completeness.

Lines and Spaces

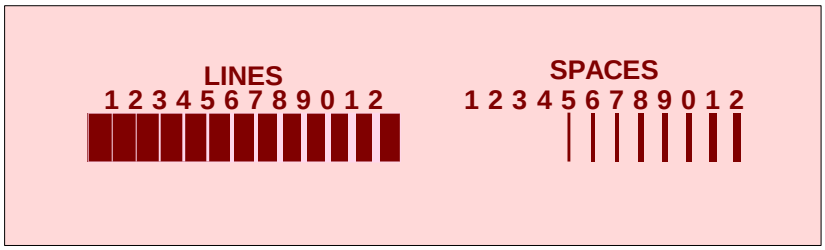
- Designed to aid in determination of development completion
- Each mask contains a set of lines and spaces which should appear aligned under the set from the previous mask
- Can also be used to determine etch level (overetch or underetch) in the same manner.
- Colors will be reversed when checking etch level. This is because oxide will appear dark red and bare silicon will appear almost white.
- Smaller lines and spaces may appear darker in color. This is ok and is most likely caused by viewing the features at a slight angle.
- Generally, as long as both the 2μm line and space is present in the corners and center of your wafer development is sufficient to proceed with etching.



* Note that actual colors will be reversed when checking etch level.

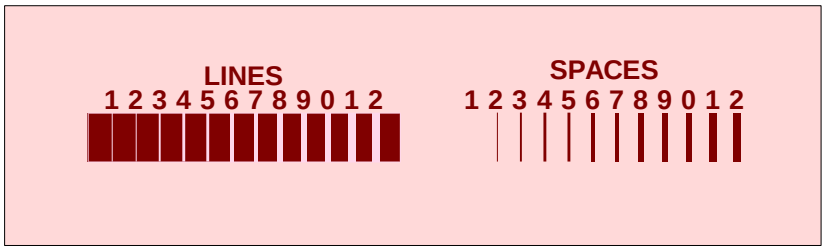
Severe Underdevelopment

- Several spaces are missing
- Smaller features have not been developed yet
- Return to developer for additional development before etching



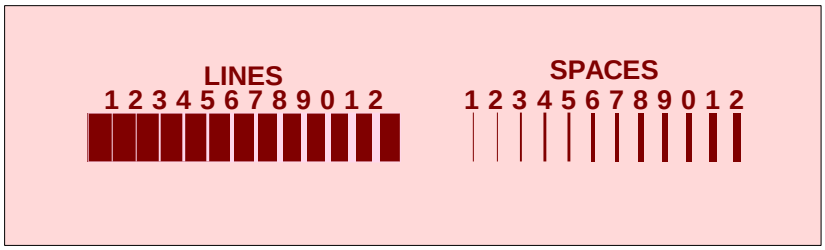
Slight Underdevelopment

- 1µm space is missing
- Acceptable level of development
- Ready to etch



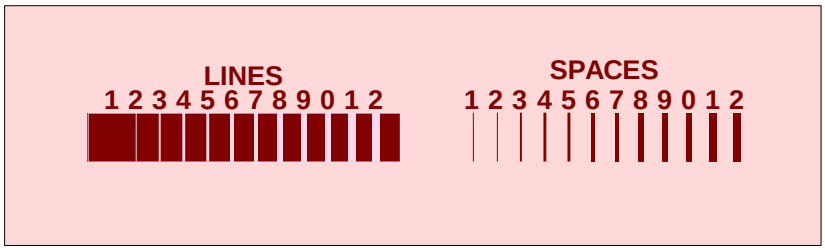
Perfect Development

- All lines and spaces present
- Ready to etch



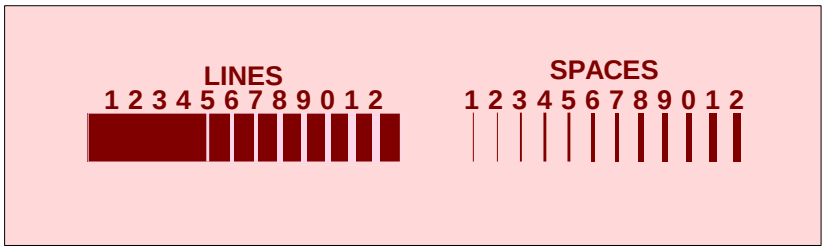
Slight Overdevelopment

- 1μm line is missing
- Acceptable level of development
- Ready to etch



Severe Overdevelopment

- Several lines are missing
- Smaller features have been erroneously removed
- Strip PR, reapply, and attempt proper development again



Appendix E - Hot Point Probe

A basic electrical property of semiconductor materials is their type of conductivity, i.e., whether the majority carriers are holes (p-type) or electrons (n-type). This property is very quickly and simply determined by employing the hot point probe. It is also a quick way of determining if all the oxide has been removed from a test area – if there is oxide left, there can be no current flowing from the sample to the probes.

The free carriers in a semiconductor behave in some ways as a gas of charged particles (a plasma). Just as heat makes a gas expand (PV=nRT), the hot point makes carriers expand away from the contact point. The charge of the dominant carrier species (electrons or holes) determines the direction of the net current flow.

A small component of the net current may be due to the heat reducing the probability that carriers remain confined spatially around their associated dopant atoms, but room temperature is so high (above absolute zero) that virtually all dopant atoms are already "excited." The extra excitation is negligible. Carrier pair generation caused by the heating does not affect this measurement since the current components from thermally generated electron-hole pairs would cancel. Note that the measurement situation is a non-equilibrium condition.

Operating Instructions

1. Turn on the power supply. The power supply is only used to heat the probe tip on the left – there is no electrical connection to the sample.
2. Turn on the picoammeter. Make sure it's in 'Auto' scale mode.
3. Load your wafer.
   a) Move the wafer chuck all the way toward the front.
   b) Place your wafer on the chuck. Be careful not to hit the probe tips. As long as the test area is on the chuck, centering is not important. Do not bother to slide the wafer beneath the tips; it will only make it difficult to remove.
4. Probe the wafer.
   a) Use the x-y stage to position the appropriate test area beneath the probes. Plastic "spokes" on the chuck allow rotation of the wafer.
   b) Watch the probes closely as you use the green button to lower them onto the wafer. Excessive 'skating' can scratch the wafer. Control of the probe descent is enhanced if you simultaneously apply some pressure to the white button while the green button is pressed.
   Consult your instructor if you suspect the prober needs adjustment. Please do not re-adjust any of the knobs on the probe assembly unless you know how to properly reset them.

5. Interpret the reading

   a) Trace the wires to determine which direction the picoammeter is connected into the circuit. Is its positive reference input (center conductor if it uses a BNC connector) connected to the hot or cold tip? Note the red and white dots on the holders for the probe tips. These correspond to the similarly colored banana jacks.

   b) Type determination: the picoammeter registers a positive current when direct current flows into its positive reference input. We leave it up to you to decide which sign on the picoammeter's display corresponds to which conduction mechanism in the semiconductor. A constant sign on the picoammeter is sufficient – its magnitude is not. It may climb slowly as the hot point heats up, and may decrease as the wafer heats up.
   No reading means either that the circuit is open (possibly from dirty tips), the tip is not hot, or that the material is either insulating (oxide) or intrinsic (compensated). Consult your instructor if you have reason to believe that prober has a problem.

6. Remove the sample.

   a) Use the white button to raise the tips.

   b) Use the x-y stage to bring the wafer out from under the tips.

   c) Remove the wafer from the chuck. Note: a drop of water can make a wafer stick to flat surfaces with enough force that it's possible to break the wafer by lifting it straight up. If the wafer resists lifting, slide it off.

7. Turn off the picoammeter and power supply unless someone else is going to use it next. Since the tips are so close, continuous heating may warm up the "cold" point and reduce the sensitivity of the apparatus, but the main reason for turning off the power supply is that we don't have a spare heater. So don't skip this step!

Appendix F - Four Point Probe

Introduction

Resistivity (ρ) is a particularly important semiconductor parameter because it can be related directly to the impurity concentration of a sample; see GT section Figure GT-1. These plots have been determined experimentally and are specifically valid for homogeneous single crystals of Silicon at room temperature (300 K). The four point probe is the apparatus typically used to determine bulk resistivity, and in conjunction with plots like GT-l, permits one to ascertain the impurity content of a given sample.

Note that the mobility of the carriers depends upon temperature, crystal defect density, and all impurities present. If your sample differs in these respects from that used to determine the empirical GT-1 curves, the actual dopant concentration you determine will only be close, not exact. Hall effect measurements can determine the mobility of the carriers in a given sample to allow for more accurate dopant concentration measurements, but Hall measurements are usually destructive to the sample. We'll use the GT-1 curves.

Theory of Operation

$$\rho = \frac{(2\pi s)V}{I} \quad (1)$$

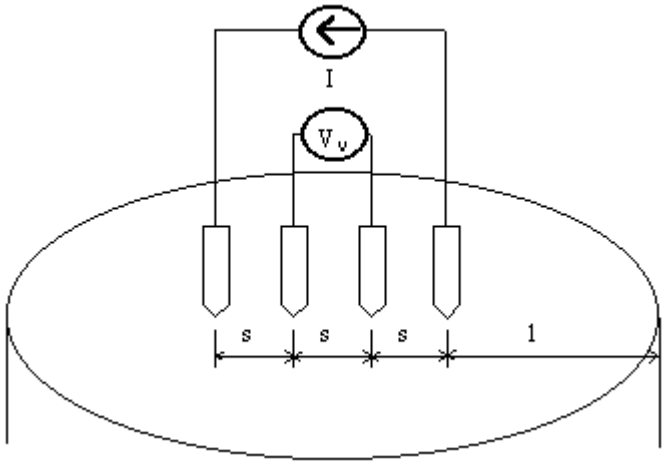


Figure 1

The subscript o in the preceding equation indicates the measured value of the resistivity and is equal to the actual value, ρ, only if the sample is of semi-infinite volume. Practical samples, of course, are of finite size. Hence, in general, $\rho \neq \rho_o$. Correction factors for six different boundary configurations have been derived by Valdes.(1) These show that in general if l, the distance from any probe to the nearest boundary, is at least 5s, no correction is required. For the cases when the sample thickness is ≤ 5s, we can compute the true resistivity from

$$\rho = a 2\pi s \frac{V}{I} = a\rho_o \qquad (2)$$

where a is the thickness correction factor which is plotted on page GT-2. From an examination of the plot we see that for values of t/s ≥ 5 the corresponding value of a is unity. Thus for samples whose thickness is at least 5 times the probe spacing, no correction factor is needed. Typical probe spacings are 25-60 mils and the wafers used in most cases are only 10-20 mils, so unfortunately we cannot ignore the correction factor. Looking again at the plot, however, we see that the curve is a straight line for values of t/s ≤ 0.5. Since it is a log-log plot the equation for the line must be of the form

$$a = K\left(\frac{t}{s}\right)^m \qquad (3)$$

where K is the value of a at (t/s) = 1, and m is the slope. Inspection of the plot shows that in this case m = 1. K is determined to be 0.72 by extrapolating the linear region up to the value at (t/s) - 1. (The exact value can be shown to be 1/(2ln2).) Hence for slices equal to or less than one half the probe spacing

$$a = 0.72\ t/s$$

When substituted into the basic equation we get:

$$\rho = a 2\pi s \frac{V}{I} = 4.53t \frac{V}{I} \quad \text{for } t/s \leq 0.5 \quad (4)$$

All samples used in the lab satisfy the one-half relationship so the above formula can be used to determine ρ. Resistivity measurements will be performed on the starting material for each experiment. The value of ρ obtained will be referred to as the bulk resistivity, and the units are Ω-cm.

If both sides of Equation (4) are divided by t we get

$$Rs = \rho/t = 4.53\ V/I \text{ for } t/s \leq 0.5 \quad (5)$$

which we refer to as sheet resistance. When the thickness t is very small, as would be the case for a diffused layer, this is the preferred measurement quantity. Note that Rs is independent of any geometrical dimension and is therefore a function of the material alone. The significance of the sheet resistance can be more easily seen if we refer to the end-to-end resistance of a rectangular sample. From the familiar resistance formula

$$R = \rho\, l/wt \quad (6)$$

we see that if w = l (a square) we get

$$R = \rho/t = R_s$$

Therefore, Rs may be interpreted as the resistance of a square sample, and for this reason the units of Rs are taken to be Ohms per square or Ω/□. Dimensionally this is the same as Ω, but this notation serves as a convenient reminder of the geometrical significance of sheet resistance.

So far in our discussion of resistivity measurements we have assumed that the size of our sample is large compared to the probe spacing so that edge effects could be ignored. This is usually the case for the bulk resistivity measurement. However, the sheet resistance measurements made in lab will be made on a "test area" of the wafer. The test area dimensions (nominally 2.9 by 5.8mm) are not that large compared to the probe spacing (25 mils). In order to get accurate measurements a correction factor for edge (geometry) effects must be included. The figure on page GT-3 gives the correction factors for two common sample geometries.

In general then

$$R_s = C\, V/I \quad (7)$$

where C is the correction factor.

Note that for d/s > 40, C = 4.53, the value we had as the multiplier in Equation (5).

References

Valdes, L. G., Proc. I.R.E., 42, pp. 420-427 (February 1954).

Smits, F. M., "Measurements of Sheet Resistivity with the Four-Point Probe," BSTJ, 37, p. 371 (1958). (Same as BT Monograph, 3894, Part 2).

The VEECO Four Point Probe

The Veeco four point probe provides a constant current which flows between two outer probes and then measures the voltage across the two inner probes to obtain the fundamental V/I parameter.

For the bulk resistivity measurement, the relevant formula is

$$\rho = 4.53\ t\ V/I$$

For sheet resistance measurements the formula is

$$Rs = C\ V/I$$

and the measured V/I value is multiplied by C (this value is already set on the probe). Refer to Fig. GT.3 for correction factor determination, but divide the number by 4.53 for the Veeco. The probe spacing S is 25 mil.

The Veeco can penetrate thin insulating surface layers by applying a short 170v pulse to the probe tips when the PENETRATE function is selected. Then, after making the resistivity measurement, the unit can determine the type of the semiconductor. For low resistivity samples the type is determined by applying an ac signal between two probes and monitoring the dc bias of the wafer with a third probe. Lightly doped semiconductors will form rectifying contacts with the probe tips causing the wafer bias to go up (positive) for N type material and negative for P type material. Highly doped semiconductors will not develop a conclusive wafer bias, but the applied ac signal can heat such material sufficiently for observation of the thermoelectric effect (as in the hot-point probe). If neither method is conclusive, both N and P indicators will flash.

Note: The electronics does not always know when the tests for conductivity type are inconclusive. If it disagrees with the hot point probe, disregard it.

Operation

1. For Bulk Resistivity: press <SLICE RES> and dial in the wafer thickness (including the units!)
2. For Sheet Resistance: press <SHT. RES> and dial in the posted geometry correction factor.
3. For V/I ratio: press <V/I>.
4. Press the <Type Auto> button in.
5. Lift cover and place wafer on the glass plate. Center the 4 probes in the test area by lowering the probes (depress bar in front manually) until they are just above, but not touching, your wafer. Adjust the glass plate until your test area is centered.
6. Lower the probes by depressing the bar in front manually. Press <RETEST> until you get two consecutive readings that are the same with the possible exception of the least significant digit. Record the values. If different from the 1st value, average the two numbers.

7. With the probes still held down, press <REV. CURR> twice and record the values. Disagreement with the other values may mean a tip is bent or a poor contact exists. 10% agreement is acceptable.
8. Average the four measurements. Note that the readings are in mΩ, Ω or kΩ as per the LEDs on the display. If measuring Rs, units are (m,K) Ω/□.
   If measuring ρ, units are (m,K) Ω-cm.

Appendix G - Lindberg/Tempress 8500 Furnace

Introduction

The Lindberg/Tempress 8500 dual stack furnace bank is a precisely regulated high temperature furnace used for multiple purposes in the laboratory. Each of the chambers (eight total) is dedicated to a particular function to minimize cross contamination (especially of dopants).

Temperature Range

The furnace is capable of regulating temperatures up to 1350 ±0.1°C (at equilibrium)., although the normal operating range is 400°C to 1100°C. The furnaces are kept at either 400°C (solid source chambers) or 600°C (oxidation/drive chambers) during standby, and temperatures of 950°C (boron predep), 1000°C (gate oxidation and phosphorus predep), and 1100°C (field oxidation, boron drive) during operation. These temperatures where selected based on the conditions of fast cycle time to operating temperature, dopant source reproducibility, and chamber longevity. A higher temperature standby condition is not utilized because the life of the furnace core windings decreases rapidly at elevated temperatures. The furnaces are not completely shut off when in standby, or raised to higher temperatures during use, because cycling of temperature below 275°C or above 1100°C devitrifies (crystallizes) the quartz tubes.

Chamber Material

The material used for the chambers where the processes occur must meet two important criteria: 1)the ability to withstand large thermal gradients and 2) material compatibility with the silicon process. Thus, most chambers are made of 'quartz,' or more correctly, 'fused silica'. Fused silica is amorphous silicon dioxide (SiO_2), which exhibits a low coefficient of thermal expansion (~5x10-7mm/mm/°C) and is fully compatible when of sufficient purity, since it is the same material that is used for dopant masking.

The chambers used in the lab are stabilized high purity fused silica. Stabilized refers to the thin cristabolite, or crystalline, layer around the circumference of the chamber which minimizes stress fractures from thermal cycling. Purity level is ~99.97% SiO_2.

Processes

Steam Oxidation: Steam oxidation is used to form oxides used for dopant masking. The steam is created pyrogenically, e.g. through the combustion of oxygen and hydrogen gases. This produces a fast growing oxide which is ideal for diffusion masking,

although its electrical properties are compromised due to a more porous structure with a higher incorporation of mobiles charges compared to dry oxide.

Dry Oxidation: Dry oxidation (used for the gate dielectric of MOS devices) is accomplished using only pure oxygen. This produces a dense oxide with low pinhole density, high breakdown voltage, and low incorporated mobile charge.

Boron Doping: Boron doping utilizes solid 4" diameter disc-type sources composed of BN (boron nitride). BN is an inert ceramic with a low vapor pressure, so it must be conditioned to act as a proper dopant source. Prior to use the solid sources are oxidized to form a B_2O_3 layer. It is the oxide which has a significant vapor pressure at the diffusion temperatures. B_2O_3 reacts with silicon to form SiO_2 with an extremely high concentration of boron – BSG (borosilicate glass).

Phosphorus Doping: Phosphorus doping utilizes solid 4" diameter disc-type solid sources composed of SiP_2O_7 in a fine SiO_2 matrix. The SiP_2O_7 decomposes at diffusion temperatures to form P_2O_5, which vaporizes and reacts with silicon to form PSG (phosphosilicate glass). No conditioning (other than an 8 hour soak at the process temperature) is required as with the BN wafers since it is a decomposition reaction that creates a volatile oxide.

The furnace is divided into two sides: manual loading and autoloading. This arrangement allows you to experience first hand the advantages and disadvantages of both types of systems.

Control

The furnaces are controlled either by a Digital Temperature Controller (DTC) on the manual side, or a combination of a DTC and a Digital Process Controller (DPC) on the autoloader side.

DTC: The DTC is a PID (Proportional, Integral, Derivative) controller, which in simplest terms means that the temperature can be ramped extremely fast with no overshoot, allows for quick recovery during thermal loading (loading in a cool boat full of wafers), and very stable setpoint temperature maintenance (±0.1 °C deviation).

The input for the temperature control comes from two types of thermocouples: spike and paddle. There are three type R spike thermocouples on the outside surface of the chamber, located in the center of each heating element (source, center, and handle). These are used during the normal operation of the furnace, although the temperature read by the TCs is different from the actual temperature that the wafers (inside the chamber) are at. There is also one type BX paddle thermocouple which is inserted inside the chambers. This TC is used to calibrate the setpoints required for the spike TCs to achieve the desired temperature on the inside of the furnace. The paddle TC can also be used to control the furnace temperature once it is inside the chamber.

DPC: The DPC is used in conjunction with the DTC on the autoload side of the furnace. Its function is to allow for automation of the furnace since there are more operations going on other than just temperature control. The DPC consists of a microprocessor interfaced with analog and digital inputs and outputs.

The digital inputs currently are used for location setpoints for the cantilever loading system. The digital outputs are used for the control of the stepper motors in the loading system. Currently, the analog I/O is not used, but will be used in the future for control of mass flow controllers (MFCs). The digital outputs can also be used for control of additional equipment, and will be used for solenoid valves in the future.

The DPC is also the master of the DTC when the two are connected, disabling manual setting of temperature through the DTC. The DPC will set the correct temperature recipe in the DTC based on the program input into the DPC.

The DPC can contain up to 16 programs which are input through a simple programming recipe.

Overtemp Modules: The furnace is also equipped with overtemperature detection which prevents accidental melt down of the quartz chambers in the event of equipment failure. There are three TCs per chamber which provide redundancy to the spike TCs - if the temperature rises above the overtemp setpoints, the system will trip off the circuit breakers supplying power to the individual furnaces.

Hydrogen: To create pyrogenic steam, hydrogen and oxygen are combusted in the chamber. The presence of hydrogen and oxygen together can be a potentially dangerous situation, but is minimized with proper interlocks. The furnace gas delivery system is interlocked to prevent the introduction of hydrogen if two criteria are not met:

low temperature: the furnace temperature must be >800°C for spontaneous combustion

gas ratio analyzer: the quantity of hydrogen is greater than the stoichiometric ratio required for complete combustion of hydrogen

A hydrogen gas detection system is also present to detect any potential leaks or failures of the interlocks. There are three monitoring points designed to detect the presence of gas when it exceeds 5% LEL (lower explosion limit). This system is connected to a local alarm system which is activated by the low alarm (5% LEL) to warn of a potential release. If the high alarm (10% LEL is activated, the system will sound the building alarm to provide for evacuation and the notification of the fire department.

Furnace Loading: Manual

The ECE 444 diffusion furnaces are very much like those described in Appendix H of Anner's Planar Processing Primer. Refer to it for construction details. The following instructions are for manual operation, however.

CAUTION: Quartz hot enough to severely burn does not necessarily look any different than cool quartz. Quartz is also extremely expensive and can be ruined by contamination. The 6" furnace tubes cost over $1000, the boats over $200. The worst thing a student can do is to knowingly spread contamination from, say a small piece of burned glove on a boat, to the other quartzware and, consequently, to the wafers of classmates. If you suspect accidental contamination, notify the instructor immediately! Do not worry about your letter grade.

1. Verify that the furnace is at the proper temperature for the processing step by checking the temperature setting on the Digital Temperature controller for the chamber you are using.
   a) If the actual temperature (TA) of the three zones is not displayed, press the following keys:
      i) <clear and display>
      ii) <temp>
   b) You can check individual setpoints (SP) and actual temperatures (TA) by pressing:
      i) <1> = handle
      ii) <2> = center
      iii) <3> = source
      iv) <0> = all three zones (default)
2. Check that the gas panel power is ON and that it is in the MANUAL mode.
3. Check that only nitrogen is flowing in the furnace.
4. Put on the high temperature gloves over your latex gloves. Open the scavenger hood door and carefully remove the end cap. Place it on the stainless steel counter in front of the opposite bank of furnaces so it's well out of the way. Be quick, it's very hot.
5. Put on the high temperature gloves and unload the boat from the mouth of the chamber.
6. Carefully place the boat on the quartz plate located on the stainless steel table.
7. Remove the high temperature gloves.
8. Load your wafer into the boat.

If doing a predep, the wafer should face the nearest source wafer. Otherwise it should not matter, but note which way it is loaded as a matter of good scientific practice. In the case of predeps, use the diagram below to determine the boat position of your wafer for the electronic logsheet entry. It will help if you observe the dimensions of the boat now since you will have to hook it at a considerable distance without damaging the wafers later. Dummy wafers are used in all the boats not only for protection from the pull rods, but because the first and last wafers experience different gas flow conditions.

9. Put on the high temperature gloves.
10. Reload the boat into the mouth of the chamber.
11. With the high temperature gloves, use the appropriate long pull rod to slowly push the boat until the tape mark is flush with the scavenger hood face. Each furnace has its own long pullrod.
12. Allow the pull rod to cool for several seconds before returning it to the quartz storage tube.
13. Switch gases as the recipe dictates.

Furnace Unloading: Manual

The unloading procedure is basically the same with the obvious differences that the long pull rod must be used to retrieve the boat from the center of the furnace and wafers will be removed from the boat.

1. Put on the high temperature gloves over your latex gloves.
2. 30 second slow pull. Pull the boat to the mouth of the furnace using the long pull rod for that furnace.

   Depth perception helps a great deal in hooking the boat when it's in the middle of the furnace. Remember, the boat was left where the tape lined up with the face plate. It may help to gently touch the boat without lifting the pullrod in order to calibrate the depth. It also helps to use the end of the furnace tube as a fulcrum and pivot the hook upward as you hook the boat. Avoid touching the wafers with the rod. Pulling too fast will result in an abnormally high sheet resistance because a significant number of atoms will be frozen off lattice sites, making them inactive.
3. Allow the pull rod to cool for several seconds before returning it to the quartz storage tube.
4. Use the lifting fork to move the boat to the quartz disc. Leave the fork in the boat.
5. Unload the boat. Remember, it's hot!

   Hold the wafers in air for 10 seconds or so to cool before placing them into the plastic wafer carriers. Although wafers cool very fast, the quartz boat will retain heat and keep wafers hot for a relatively long time. What implications does this have on the "real" diffusion time?
6. Reload the boat into the mouth of the chamber using the lifting fork and high temperature gloves.

Autoload Processing

To run the process recipe for the autoloader side of the furnace, press the following keys on the DPC:

1. <clear and display> repeatedly until DISPLAY 'PROCESS NAME' appears (where 'PROCESS NAME' = BORON DRIVE, PHOSPHORUS PREDEP, or GATE OX)
2. <run/halt>
3. Make sure the display says EMPTSTMCN1 RUN? If not, press:
   a) <recipe>
   b) <1>
   c) <enter>
   d) <clear and display>
   e) <run/halt>
4. The display should now read EMPTSTMCN1 RUN?
5. <enter>

The process is totally automatic for the Phosphorus Predep. Additional steps must be taken for the Boron Drive:

1. When the elephant and boat are fully loaded into the chamber the display will read: START GASES
2. As soon as this is displayed, flow your gases as specified in the lab manual and begin timing.
3. When the process is complete, press <clear and display>
4. Press <run/halt>
5. Press <enter>

The furnace will then continue the recipe and unload.

Appendix H - Ultratech 1000WF Stepper

Introduction

The Ultratech 1000 Wide Field steppers are the latest addition to lithography in the ECE444 lab. They are highly automated, extremely complex machines which have replaced the manual contact aligners. There actually was a reluctance to install these machines due to their cost and the removal of operator involvement with aligning.

The 1000WF is still in use by major semiconductor fabs (such as the former AC Delco) and were in use by Intel until December of 1996. There are enough left to support third party parts suppliers and reconditioners. They are ideal for start-up companies desiring reasonably priced photolithography tools for non-critical, lower resolution processes with mix-and-match capabilities with other steppers.

The steppers present in the lab have been modified by Intel, and their performance has been enhanced from stock machines. Positioning resolution has been increased (closer alignment), and the optics have been enhanced (possible to achieve submicron resolution).

System Information

The operation of the steppers is very exact (presently there are approximately 4 manuals, 14 hours of setup video, and 15 VHS videos covering operation and maintenance in the 444 library). Therefore a short overview is all that will be presented.

Positioning System

To provide for accurate positioning, the 1000WF consists of two stepper motors with feedback from a Zeeman split HeNe laser interferometer. Laser interferometers work through the counting of interference fringes created as a laser beam is reflected back onto itself. As the stage moves, the distance the laser traverses changes, and the phase of the beam upon reflection changes, resulting in a maxima and minima of brightness as the beam destructively and constructively interferes with itself. Each fringe signifies a specific distance based on the operating wavelength of the laser. As the fringes move, a counter determines the number of fringes which pass through an aperture, and can correlate that with a specific distance. This distance is used to provide an absolute position of the mirrors mounted on the stage with respect to a home position. The home position is determined by a limit switch.

By implementing two mirrors and splitting the laser beam, a very accurate position of the stage can be determined for both the X and Y-axes.

The interferometric determination of stage position is used to drive two stepper motors for stage placement. The stepper motors drive pinch rollers which propel the air bearing supported stage along guide rods.

Exposure System

The 1000WF consists of a very simple but effective 1:1 image projection system. A mercury arc lamp is used for the UV source utilizing the g- and h-lines (the i-line is filtered out because the epoxy used in the optical system decomposes with exposure to that wavelength). The beam is projected through a light pipe, an actinic filter ('actinic' means 'active', so it filters out the 'active' UV components for alignment), through a reticle (mask), is redirected by a prism through a lens doublet, reflected back by a mirror, back through the doublet, and finally through another prism to the wafer. See Figure H1.

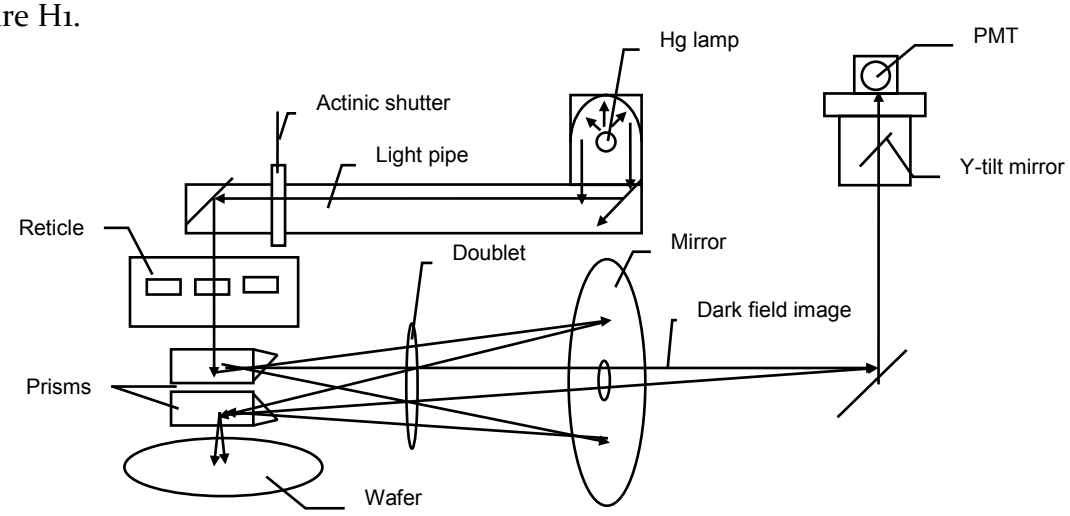


Figure H1. 1000WF light system.

The PMT and Y-tilt mirror are used for pattern recognition and alignment using the darkfield image from the wafer.

Registration

One of the most important aspects of lithography is registration. The 1000WF determines position of the mask in relation to the existing wafer pattern both mechanically and optically in a multistage process.

The first mask of the process exposes the pattern onto the wafer in blind step mode. Blind stepping is a purely mechanical alignment, and relies on the interferometer for placement of the individual die. This first mask level contains several alignment targets which will be used by subsequent mask levels.

There are four types of mechanical alignment used in the 1000WF; they are listed in order of operation:

1. ***Flat find***: used for rough theta adjustment
2. ***Bash routine***: used to center the wafer on the chuck
3. ***Wafer edge detection***: used to center the wafer under the optics
4. ***Reticle guides***: used to locate the reticle in the y-axis; must be <75µm misaligned to reticle fiducial, there is no y-axis adjustment

Optical Alignment

There are three types of optical targets/keys used in the 1000WF:

1. ***Reticle alignment fiducial***: used for absolute positioning of the mask to the optical system; this is the first optical registration routine, used when loading a reticle for the current mask level – see Figure 2.

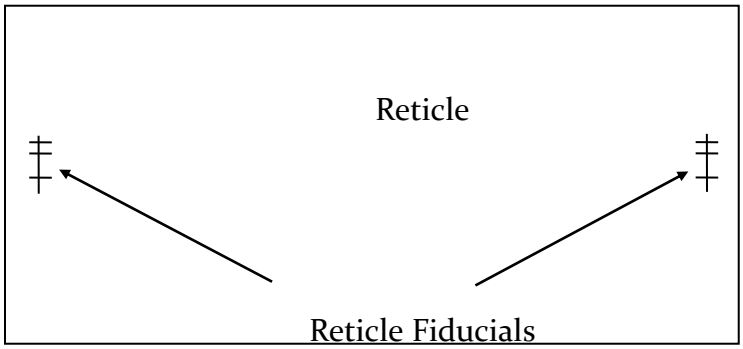


Figure 2: Reticle Alignment Fiducials

2. ***Optical alignment target (OAT):*** large target used for global positioning of the wafer in relation to the mask pattern; aligns wafer to reticle to within 10µm; this routine is performed when a wafer is loaded under the optics and all mechanical alignments have been performed – see Figure 3.

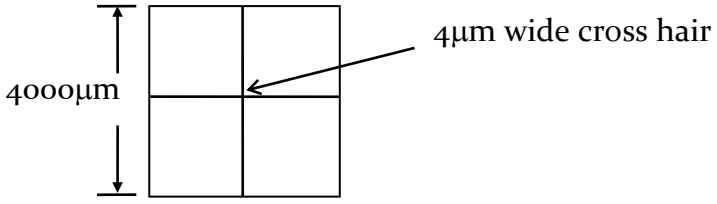


Figure 3: Optical Alignment Target (OAT)

Horizontal Alignment Marks (HAMs): used for fine alignment and theta (rotational) adjustment; aligns wafer to reticle to within <1μm; this routine is performed after the OAT is found – see Figure 4.

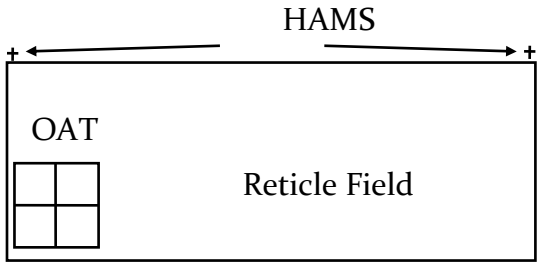


Figure 4: Horizontal Alignment Marks (HAMS)

The Reticle

Contact aligners use a mask which covers the entire area to be exposed (Figure 5). This method of exposure has several disadvantages as they become larger:

- large masks are cumbersome and are more prone to breakage
- difficult to clean and inspect
- larger area for particles to land, causing pattern defects

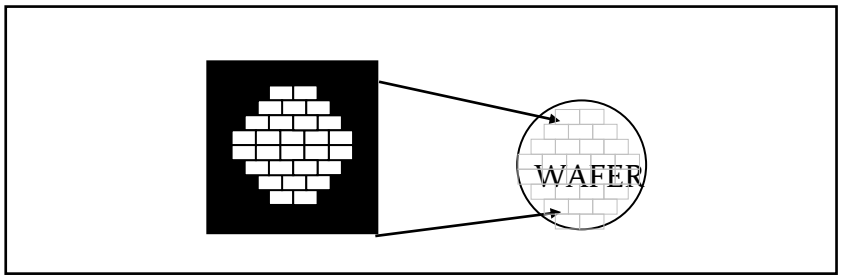


Figure 5: Contact aligner mask.

A stepper, on the other hand, utilizes a field instead of the entire mask pattern (Figure 6). The field is a subset of the desired image to be transferred to the wafer. This field is stepped and repeated over the wafer. Below is a diagram of the reticle (with 3 fields) used in the 1000WF:

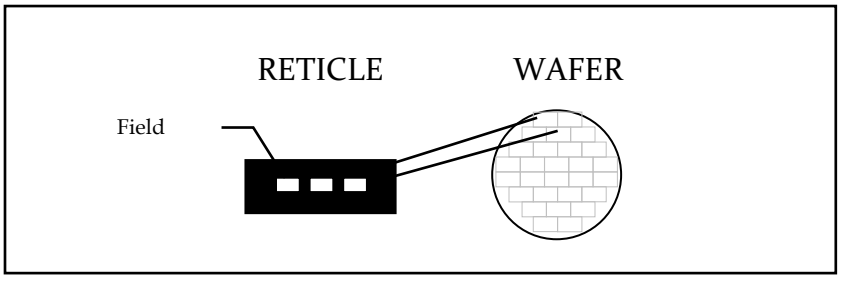


Figure 6: Stepper reticle.

The advantages of the reticle are:

- smaller, therefore easier to handle
- less area for particles to cause defects
- same image for every device on the wafer (can be a disadvantage)
- versatile - image pattern can be changed through software
- allows for drop-ins (test patterns, different devices) which can be temporary

Although there are several advantages to the reticle, there are also disadvantages:

- same image for every device on the wafer (propagation of faults)
- mechanical alignment of guide structures critical
- registration targets/keys critical
- can be more expensive (labor intensive – additional post processing steps)

Reticle Layout

A complete reticle is more complex than a contact mask. Below is a diagram of the features explained above:

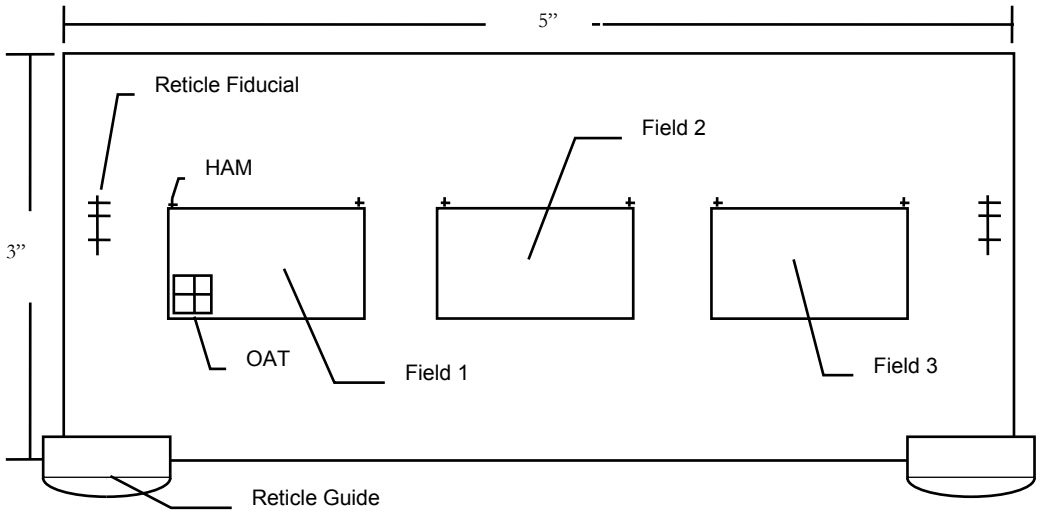


Figure 7: UltratechWidefield Reticle Layout

Operation

Although the steppers are complex to set up, they are very easy to run. The stepper will be warmed up prior to class.

Load the Reticle

The reticle contains three fields, each corresponding to a mask level (see Figure 8.). This requires the use of two reticles to obtain the entire mask set.

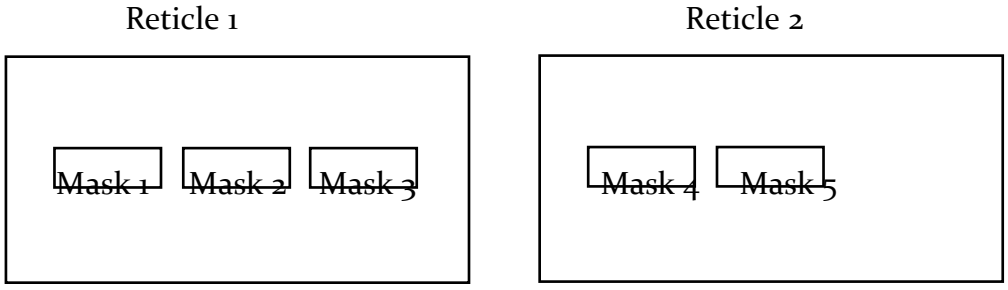


Figure 8: Mask locations.

The mask used is determined by the *reticle data* loaded into the stepper. The *reticle data* is an array of data that contains all the physical characteristics of the stepper, reticle, fields, and wafer.

The reticle must not be changed by students! If you require the use of a reticle not in the stepper, contact your TA.

You will have to change *reticle data* to align and expose with the correct mask level.

Load Reticle Data

1. Press <**K1**> (*Load/Unload Reticle*)
2. If a Reticle is loaded, proceed to 3. If the reticle is not loaded, proceed to 4.
3. If a reticle is loaded, it will ask '***Unload the reticle?***'
   a) press <**y**> (*yes*)
   b) The reticle will unload.
   c) After unloading, make sure that the reticle is seated properly in its guides by pushing it gently to the right and tilting the left side up about ¼" and gently letting it back down.
   d) Press <**K1**> when the stepper returns to the main menu and proceed to 4.
4. If there is no reticle loaded, the stepper will ask '***Load reticle data?***'
   a) Make sure that the reticle is seated properly in its guides by pushing it gently to the right and tilting the left side up about ¼" and gently letting it back down.
   b) Insert the reticle data disk

c) press <**y**> (*yes*)

d) The stepper will ask '***Input reticle data file name***'

e) Type in the mask level name:

Step	Mask level name
PR1 -	layer1
PR2 -	layer2
PR3 -	layer3
PR4 -	layer4
PR5 -	layer5

5. press <***ENTER***>: the HP200 will load the data into memory
6. The stepper will ask '***Load reticle?***'
   a) Place the frosty wafer (the unpolished side of an unused wafer) into the autoloader.
   b) press <**y**> (*yes*)
   c) The reticle will go through a series of tests to line it up properly with the optics. If it should fail reticle load, contact the TA.
   d) Remove the frosty wafer from the autoloader after successful loading of the reticle.

Align and Expose Wafer

After successful completion of reticle load, the HP200 will bring up the run mode screen. Run mode determines the method of alignment and exposure.

1. For layer1, proceed to 2. For all other layers, proceed to 3.
2. For layer1, the stepper will perform a blind step. Blind stepping is the mechanical alignment of the reticle to the wafer using only the interferometer as a means of registration.
   a) press <**1**> (*run mode 1 - mechanically align and expose*)
   b) The stepper will ask '***Input exposure intensity***'
   c) type in <**150**> (*150mJ/cm²*)
   d) press <**ENTER**>
   e) The stepper will ask '***Exposure is 150. Ok?***'
   f) type <**y**> (*yes*)
   g) The stepper will say '***waiting to load wafer***'
   h) Load your wafer into the autoloader by placing it with tweezers into the left side of the autoloader. Place the wafer so that it rests both on the red circle and the drive belts.
   i) The wafer will automatically load onto the chuck after the flat find routine, and will be aligned and exposed automatically.

j) After successful alignment and exposure, the wafer will be returned on the right side of the autoloader. Remove it and place it back into your wafer container with tweezers.

k) The stepper will say, '***waiting to load wafer'.*** If there are others waiting to expose the same mask, they may continue without reloading the reticle.

3. For all layers other than layer1, the stepper will align wafer targets through reticle keys optically.

a) press <**2**> (*align and expose*)

b) The stepper will ask '***Input exposure intensity***'

c) type in <**150**> (*150mJ/cm²*)

d) press <**ENTER**>

e) The stepper will ask '***Exposure is 150. Ok?***'

f) type <**y**> (*yes*)

g) The stepper will say '***waiting to load wafer***'

h) Load your wafer into the autoloader by placing it with tweezers into the left side of the autoloader. Place the wafer so that it rests both on the red circle and the drive belts.

i) The wafer will automatically load onto the chuck after the flat find routine, and will be aligned and exposed automatically.

j) After successful alignment and exposure, the wafer will be returned on the right side of the autoloader. Remove it and place it back into your wafer container with tweezers.

k) The stepper will say, '***waiting to load wafer***'. If there are others waiting to expose the same mask, they may continue without reloading the reticle.

Appendix J - The Test Stations

The purpose of a prober is to make electrical connections from the micro-world of the wafer to the macro-world we live in. The typical probe pad on the ECE444 mask set is 100μm on a side, which would be quite difficult to solder or otherwise make connections by eye. This is not easy considering that solder does not wet aluminum, requiring a second metallization using a different metal.

Making contact to the wafer is therefore left to the micromanipulators with very fine tungsten probe tips (25μm radius). Positioning of the probes requires the use of a stereozoom microscope and takes practice (which is why you are here!).

Be careful with the probers! They are extremely precise instruments, as the cost proves it.

Do not:

- lower the probes onto the wafer with too much force (this will curl or 'fish hook' the sharp points)
- overextend the micromanipulators (they will bind). If you feel any ***resistance*** at all ***stop***!
- lower the probe stage with the probes down (a good way to 'fish hook' the tips)
- open the chuck vacuum without a wafer (causes excessive blow-by on the house vacuum)
- move the base of the micromanipulators (they have been setup for ease in probing)
- change the SMU leads to the probes
- leave the probe stage down when not in use

Use of the probes

- Place your wafer on the wafer chuck
- Turn on the chuck vacuum switch.
- Raise each of the probes a couple of turns with the ***UP*** positioner (top knob).
- Lower the probe stage slowly with the lever on the left hand side.
- If any of the probe tips look like they will touch the wafer before the stage is completely down, raise the tips and continue lowering the stage.
- Repeat until the stage is fully lowered with none of the probes touching the wafer.
- Turn on the microscope light – you will only need about 75% power. The lower the power, the longer the bulbs last.

- Move the first device to be tested to the center of the microscope field of view using the stage's X and Y controls (located at the front of the stage).
- Carefully make contact to the device pads with the probes using the X, Y, and Z controls of the micromanipulator – ***Do not use the probe bodies!***

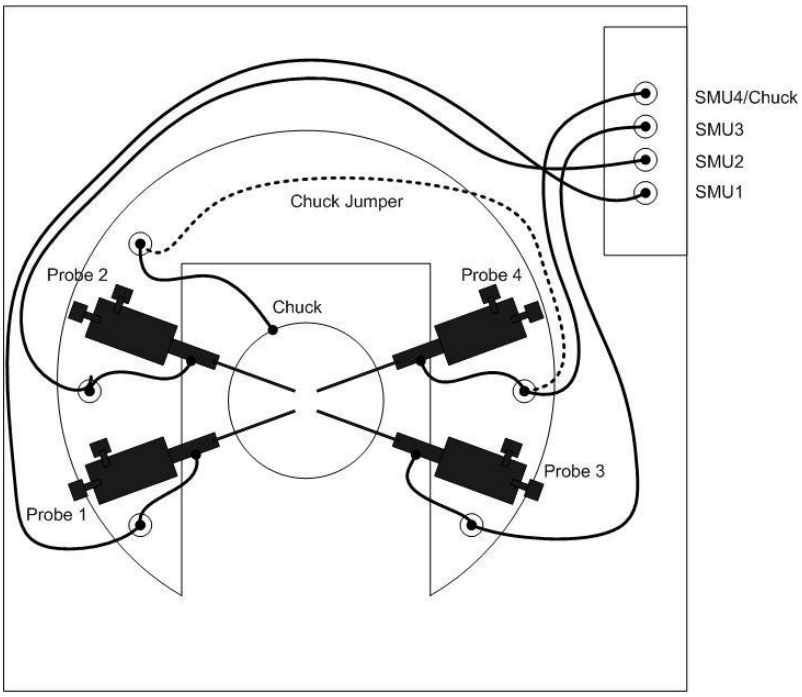
Electrical connectors

Probes 1, 2, 3, and 4 are connected to the first four switches on the side panel of the probe station's cover. These switches determine which instrument will be connected to the probe tip:

UP - HP parameter analyzer

DOWN - HP LCR meter

Probe 4 also has provisions for a jumper so that the chuck may be connected to the SMU cables. Please check to make sure that the jumper is connected to the appropriate contact device!



The most common mistake when testing devices is having the wrong instrument connected to your probe. I-V measurements are performed by the ***Semiconductor Parameter Analyzer*** (switch ***UP***); C-V measurements are performed by the ***LCR Meter*** (switch ***DOWN***).

Probing multiple devices

When probing several similar devices, the probe stage can be raised, allowing the next device to be positioned, and then carefully lowering the stage to make contact with the new device.

Appendix K - Semiconductor Acronyms

AES: Auger emission spectroscopy; Auger electron spectroscopy

AFM: atomic force microscopy

AHU: air handling unit

Al: Aluminum

ALCVD: atomic layer chemical vapor deposition

ALD: atomic layer deposition

ALE: atomic layer epitaxy; application logic element

ANSI: American National Standards Institute

APCVD: atmospheric pressure chemical vapor deposition

aPSM or **APSM:** attenuating phase shift mask

Ar: argon

AR: aspect ratio

ARC: antireflective coating

ArF: Argon Fluoride (excimer far UV laser emitting at 193 nm wavelength**)**

As: arsenic

ASIC: application-specific integrated circuit

ASTM: American Society for Testing and Materials

ATE: automatic test equipment

Au: gold

B: billion; boron

BARC: backside antireflective coating

BED: Boron Enhanced Diffusion

BEOL: back end-of-line

BGA: ball grid array

BiCMOS: bipolar complementary metal-oxide semiconductor

BILLI: buried implanted layer for lateral isolation

BIST: built-in self test

BLD: beam lead device

BOE: buffered oxide etchant

BOX: buried oxide

BPSG: boro phosphosilicate

BST: barium strontium titanate

BTAB: bumped tape automated bonding

BV: breakdown voltage

C-to-C: cassette-to-cassette

CAIBE: chemically assisted ion beam etching

CARL: chemically amplified resist lithography

CAWC: cryogenic aerosol wafer cleaning

CBE: chemical beam epitaxy

CCD: charge-coupled device

CD: critical dimension

CDA: clean dry air

CDI: collector-diffusion isolation

CDO: controlled decomposition/oxidation

CDSEM: critical dimension scanning electron microscopy

CEL: Contrast Enhancement Layer

CFC: chlorofluorocarbon

CFM: contamination-free manufacturing

CGA: Compressed Gas Association

CIC: cleanroom interface chamber

CMOS: complementary metal-oxide semiconductor

CMP: chemical mechanical planarization; chemical mechanical polishing

CNT: carbon nanotube

CoO: cost of ownership

COPS: crystal oriented pits

CRM: cost/resource model

CSP: chip-scale package

CTE: coefficient of thermal expansion

Cu: copper

CV: capacitance-to-voltage

CV-BTS: capacitance-to-voltage biased thermal stress

CVD: chemical vapor deposition

CZ: Czochralski process

DARPA: Defense Advanced Research Projects Agency (see ARPA)

DCS: dichlorosilane

DF: darkfield

DHF: dilute hydrofluoric acid

DI: deionized; dielectric isolation

DIP: dual inline package

DIW: deionized water

DLBI: device level burn-in

DLT: device level test

DLTS: deep level transient spectroscopy

DOE: design of experiments

DOF: depth of field; depth of focus

DOE: design of experiments

DRAM: dynamic random access memory

DRIE: deep reactive ion etching

DSWB: direct step-on-wafer

DUT: device under test

DUV: deep ultraviolet

E-beam: electron beam

EBIC: electron beam-induced current

EBL: electron beam lithography

ECC: error control coding

ECO: engineering change order; edge control only

ECP: electrochemical plating

ECR: electron cyclotron resonance

EDA: electronic design automation

EDS: energy-dispersive spectroscopy; electron-dispersive spectroscopy

EDX: energy-dispersive X ray

EFEM: equipment front end module

ELF: extremely low frequency

EM: Electro-Migration

EMF: electromagnetic field

EMI: electromagnetic interference

EMO: emergency off

EMP: electromagnetic pulse

EOS: electrical overstress

EPL: electron projection lithography

EPO: emergency power off

ESD: electrostatic discharge

EUV: extreme ultraviolet

EUVL: extreme ultraviolet lithography

F: fluorine

FBGA: fine pitch ball grid array

FC: flip chip

FE: finite element; field emission

FEOL: front end-of-line

FESEM: field emission scanning electron microscope/microscopy

F/I: final inspect

FIB: focused ion beam

FIFO: first-in, first-out

FOSB: front opening shipping box

FOUP: front opening unified pod

FOV: field of view

FOX: field oxide

FPGA: field-programmable gate array

FRACAS: Failure Reporting, Analysis, and Corrective Action System

FSG: fused silica glass; fluorinated silicate glass

FTIR: Fourier transform infrared

FWHM: full-width half-maximum

FZ: float zone

GCMS: gas chromatography mass spectroscopy

GSI: giga-scale integration

HARI: high aspect ratio inspection

HAZCOM: Hazard Communication Standard

HBT: heterojunction bipolar transistor

HCI: hot carrier injection

HCM: hollow cathode magnetron

HDP: high density plasma

HDP-CVD: high density plasma chemical vapor deposition

HDPE: high density polyethylene

He: helium

HEMT: high electron mobility transistor

HEPA: high efficiency particulate air

HF: hydrofluoric acid

HiPOx: high-pressure oxidation

HMDS: hexamethyldisilizane

HOSP: hybrid organic siloxane polymer (low k dielectric)

HPCVD: high pressure chemical vapor deposition

HPLC: high performance liquid chromatography

HRTEM: high resolution transmission electron microscopy

HSQ: hydrogen silsesquioxane

HTO: high temperature oxidation

HVAC: heating, ventilating, and air conditioning

I300I: International 300 mm Initiative

IC: integrated circuit; Investment Council; ion chromatography

ICB-CVD: ion cluster beam chemical vapor deposition

ICP: inductively-coupled plasma

ICW: industrial city water

IDEAL: initiating, diagnosing, establishing, acting, leveraging

IDLH: immediately dangerous to life or health

IG: intrinsic gettering

IGBT: insulated-gate bipolar transistor

IGFET: insulated-gate field-effect transistor

II: ion implant (also I2)

ILD: interlevel dielectric; interlayer dielectric

IMD: intermetal dielectric

IMEC: Inter-university Micro-Electronics Centre (Leuven, Belgium)

IP: intellectual property

IPA: isopropyl alcohol

IPL: ion projection lithography

IR: infrared

ISMT: International SEMATECH

ITO: indium tin oxide

ITRS: International Technology Roadmap for Semiconductors

JEDEC: Joint Electron Device Engineering Council

JEIDA: Japanese Electronic Industries Development Association

JI: junction isolation

JIT: just-in-time

KGD: known good die

KrF: krypton fluoride (excimer uv laser emitting 248 nm wavelength)

LCC: leaded chip carrier, lifecycle costing

LCL: lower confidence limit

LDD: lightly doped drain

LDL: lower detection limit

LDP: low density plasma

LDPE: low density polyethylene

LEC: liquid encapsulated Czochralski crystal

LEED: low-energy electron diffraction

LEL: lower explosive limit

LID: leadless inverted device

LIFO: last in, first out

LIGA: Lithographie Galvanoformung Abformung

LIMS: laser-induced mass spectrometry

LKDM: low k dielectric material

LLCC: leadless chip carrier

LOCOS: local oxidation of silicon

LPCVD: low pressure chemical vapor deposition

LPE: liquid phase epitaxy

LSE: latex sphere equivalent

LSI: large-scale integration

LTO: low-temperature oxidation (or oxide)

LTV: local thickness variation

LVDT: linear voltage differential transducer; linear variable displacement transducer; linear variable differential transformer

MBE: molecular beam Epitaxy

MCBF: mean cycles between failures

MCM: multichip module; manufacturing cycle management

MEMS: microelectromechanical system

MESFET: metal-semiconductor field effect transistor

MFC: mass flow controller

MIC: monolithic integrated circuit

MIM: metal-insulator-metal

MIS: metal insulator silicon; metal insulator semiconductor

MLM: multilevel metal

MMIC: monolithic microwave integrated circuit

MOCVD: metal-organic chemical vapor deposition

MODFET: modulation-doped field-effect transistor

MOS: metal-oxide semiconductor

MOS-C: metal oxide semiconductor capacitor

MOSFET: metal-oxide semiconductor field effect transistor

MOVPE: metalorganic vapor phase epitaxy

mp: melting point

MRS: Materials Research Society

MSDS: Material Safety Data Sheet

MSI: medium-scale integration; manufacturing support item

MTBA: mean time between assists

MTBF: mean time between failures

MTTF: mean time to failure

MTTR: mean time to repair

MW: molecular weight

N: nitrogen

Na: sodium

NA: numerical aperture

NDA: nondisclosure agreement

NDT: nondestructive testing

NGL: next generation lithography

NIST: National Institute of Standards and Technology

NTRS: National Technology Roadmap for Semiconductors

O: oxygen

OAI: off-axis illumination

OBIC: optical beam induced current

OD: outside diameter; optical density

ODS: ozone-depleting substances

OEIC: optoelectronic integrated circuit

OEM: original equipment manufacturer

OFA: oil-free air

OL: objective lens, overlay

OLED: organic light emitting diode

OMVPE: organometallic vapor phase epitaxy

OPC: optical particle counter; optical proximity correction

OSF: Open Systems Foundation, oxidation-induced stacking fault

OSG: organosilicate glass

Ox: oxide

P: phosphorous

PAB: post apply bake

PAC: photoactive compound

PAG: photoacid generator

PCB: printed circuit board

PCMP: post chemical-mechanical polishing

PCW: process cooling water

PEB: post-exposure bake

PECVD: plasma-enhanced chemical vapor deposition

PEL: permissible exposure level (limit)

PFA: perfluoroalkoxy

PFC: perfluorocompound; perfluorocarbon

PFPE: perfluorinated polyether

PGA: pin grid array

PGMEA: propylene glycol monomethyl ether acetate

PI: proportional integral

PID: proportional integral derivative; process-induced defect

PIP: process-induced particles

PLCC: plastic leaded chip carrier

PM: particle monitor; preventive maintenance; process module

PMMA: polymethyl methacrylate

PMT: photomultiplier tube

POU: point-of-use

PP: polypropylene

PPE: personal protective equipment

PPGA: plastic pin grid array

PSG: phosphosilicate glass; phosphorus doped silicon glass

PSL: polystyrene latex

PSLS: polystyrene latex sphere

PSM: phase shifting mask; phase shift mask

PTC: pre- and post-process treatment chambers

PTFE: polytetrafluorethylene; Teflon

PVA: polyvinylacetate

PVC: polyvinylchloride

PVD: physical vapor deposition

PVDF: polyvinylidene fluoride

PZT: lead zirconium titanate

QBD: charge to breakdown

QCM: quartz crystal microbalance

QDR: quick dump rinse

QFP: quad flat pack

QFPN: quad flat pack nonleaded

RBB: base sheet resistance

RBS: refractive backscattering; Rutherford backscattering spectroscopy

RF: radio frequency; resonance frequency

RFI: request for information; radio frequency interference

RFP: request for plan; request for proposal; radio frequency probe

RFQ: request for quote

RGA: residual gas analysis

RH: relative humidity

RHEED: reflecting (reflected) high energy electron diffraction

RIBE: reactive ion beam etching

RIE: reactive ion etch

RO: reverse osmosis

ROI: return on investment

RS: sheet resistance

RT: room temperature

RTA: rapid thermal anneal

RTD: resistance temperature detector

RTO: rapid thermal oxidation; regenerative thermal oxidizer

RTP: rapid thermal processing (or processor)

Sb: antimony

SBIR: Small Business Innovative Research

SC1: Standard Clean 1

SC2: Standard Clean 2

SCA: surface charge analysis

SCALPEL: scattering with aperture limited projection lithography

SCBA: self-contained breathing apparatus

SCF: super critical fluid

SCFH: standard cubic feet per hour

SCP: single chip package

SCR: silicon controlled rectifier

S/D: source/drain

SECS: Semiconductor Equipment Communications Standard

SEG: selective epitaxial growth

SEM: scanning electron microscopy; specific equipment model

SEMI: Semiconductor Equipment and Materials International

SIA: Semiconductor Industry Association

SiGe: silicon-germanium

SiLK: silicon low-k

SIMOX: separation by implantation of oxygen

SIMS: secondary ion mass spectroscopy

SiON: silicon oxynitride

SLAM: scanning laser acoustic microscopy; single layer alumina metallization

SLSI: super large scale integration

SMD: surface mount device

SMIF: standard mechanical interface

SMT: surface mount technology

SO: small outline (package)

SOC: system on a chip; silicon-on-chip

SOD: spin-on dielectric

SOG: spin-on glass

SOI: silicon on insulator

SOIC: small outline integrated circuit

SOJ: small outline j-bend

SOP: small outline gull wing

SOP: standard operating procedure

SOS: silicon on sapphire

SPC: statistical process control

SPICE: simulation program with integrated circuit emphasis

SPM: scanning probe microscopy; sulfuric acid/hydrogen peroxide mixture

SRC: Semiconductor Research Corporation

SSI: small scale integration

STEL: short-term exposure limit

STI: shallow trench isolation

STM: scanning tunneling microscopy

SWP: single wafer processing

TAB: Technical Advisory Board; tape automated bonding

TBD: time to breakdown

TC: time constant; temperature coefficient; thermocouple

TCE: temperature coefficient of expansion

TDDB: time-dependent dielectric breakdown

TEM: transmission electron microscopy; transverse electromagnetic

TEOS: tetraethoxysilane; tetraethylorthosilicate; tetraethelorthosilicate; tetrethoxysilicide

TFE: tetrafluorethylene

TFSMS: thin films stress measurement system

TFT: thin film transistors

THC: total hydrocarbon

TiN: titanium nitride

TLV: threshold limit value

TLV-STEL: threshold limit value-short term exposure limit

TLV/TWA: threshold limit value/time-weighted average

TMAH: tetramethyl ammonium hydroxide

TMP: trimethylphosphate, turbomolecular pump

TOC: total organic carbon; total oxidizable carbon

TPG: test pattern generation

TSOP: thin small outline package

UCL: upper confidence limit; upper control limit

UEL: upper explosive limit

UHP: ultra-high purity

UHV: ultra-high vacuum

ULK: ultra low-k

ULPA: ultra-low particulate air

ULSI: ultra large-scale integration

UPDIW: ultra-pure deionized water

UPW: ultrapure water

USG: undoped silica glass

USOP: ultra small outline package

UV: ultraviolet

VASE: variable angle spectroscopic ellipsometry

VCSEL: vertical cavity surface emitting laser

VDP: Van der Pauw

VHSIC: very high-speed integrated circuit

VLSI: very large-scale integration

VOC: volatile organic compound

VPE: vapor phase epitaxy

VUV: vacuum ultra-violet

WDS: wavelength-dispersive spectrometry of X-rays

WIB: within-batch

WIP: work in process; work in progress

WIW: within-wafer

WLBI: wafer-level burn-in

WLT: wafer-level test

WPH: wafers per hour

WSI: wafer-scale integration

WSPW: wafer starts per week

XPS: X-ray photoelectron spectroscopy

XRD: X-ray diffraction

XRF: X-ray fluorescence spectrometry

XRL: X-ray lithography

Appendix L - Common IC Processing Terms

50:1 Etch – 50 parts DI water to 1 part HF: *slow silicon dioxide etch used to remove native oxide.*

4PP – four point probe: *resistivity characterization tool, used to determine general doping levels of wafers/diffused areas.*

Acetone - $[CH_3]_2CO$: *a colorless, volatile, and extremely flammable liquid used as a solvent and as a reagent.* [SEMATECH]

Alignment mark: *an image selectively placed within or outside an array for either testing or aligning, or both.* [ASTM F127-84] *Also called alignment key and alignment target.*

Ammonium fluoride - NH_4F: *a white crystalline salt used to buffer hydrofluoric acid etches that dissolve silicon dioxide but not silicon. An example of such an etch is the buffered oxide etch*. [SEMATECH]

Ammonium hydroxide - NH_4OH: *a weak base formed when ammonia is dissolved in water.* [SEMATECH]

Angstrom - Å: *unit of linear measure equal to one ten billionths of a meter (10-10 m). (The diameter of a human hair is approximately 750,000 Å.) The preferred SI unit is nanometers. 10 Å=1 nm.* [SEMATECH]

Anneal: *a high-temperature operation that relieves stress in silicon, activates ion-implanted dopants, reduces structural defects and stress, and reduces interface charge at the silicon-silicon dioxide interface.* [SEMATECH]

Ashing: *process of removing photoresist with oxygen plasma.*

BN – boron nitride: *inert ceramic machined into discs used for predeposition of boron. Before use the wafers must be oxidized to form a volatile compound to transfer boron to a wafer.*

B_2O_3 – boron oxide: *volatile oxide used to transfer boron to a wafer.*

BOE – buffered oxide etch: *an extremely hazardous corrosive used to etch silicon dioxide from a wafer. This acid has a 20- to 30-minute reaction delay after contact with skin or eyes.* [SEMATECH]

BSG – boro-silicate glass: *silicon dioxide containing a large concentration of boron. Forms when B_2O_3 reacts with silicon at high temperature.*

Cassette: *an open structure that holds one or more substrates.* [SEMI E44-95]

Cleanroom: *a confined area in which the humidity, temperature, particulate matter, and contamination are precisely controlled within specified parameters. The class of the cleanroom defines the maximum number of particles of 0.5-micrometer size or larger that may exist in one cubic foot of air in the designated area. For example, a class 1 cleanroom allows one such particle of any kind to exist in one cubic foot of space; a class 10 area may contain no more than 10 such particles in one cubic foot of space.* [SEMATECH]

Coefficient of thermal expansion – CTE: *the increase in length or volume of a solid, liquid, or gas for a rise of 1 degree C at constant pressure. This coefficient is used, along with the glass transition temperature, to determine the expansion characteristics of molding compounds used in the manufacture of semiconductor packages. Usually, the linear coefficient is used for packaging considerations.* [SEMATECH]

Crystal: *a solid composed of atoms, ions, or molecules arranged in a pattern that is periodic in three dimensions.* [ASTM F1241]

Damage: 1 : *of a single-crystal silicon specimen, a defect of the crystal lattice in the form of irreversible deformation that results from mechanical surface treatments such as sawing, lapping, grinding, sandblasting, and shot peening at room temperature without subsequent heat treatments.* [ASTM F1241] 2 : *any yield or reliability detractors other than those related to design, process specification violations, or particles.* [SEMATECH]

Deep level impurity: *a chemical element that, when introduced into a semiconductor, has an energy level (or levels) that lies on the midrange of the forbidden energy gap, between the energy levels of the dopant impurity species.* [ASTM F1241]

Depletion layer: *in a semiconductor, a region in which the charge-carrier charge density is not sufficient to neutralize the net fixed-charge density of donors and acceptors.* [SEMI M1-94 and ASTM F1241] *Also called barrier layer, blocking layer, and space-charge layer.*

Design rules: *rules that state the allowable dimensions of features used in the design and layout of integrated circuits; rules unique to a specific process technology (including limits for feature size, feature separation, layer-to-layer overlap, and layer-to-layer feature separation).* [SEMATECH]

Developer: 1 : *equipment that uses liquids to remove exposed positive resist from wafers or substrates.* [SEMATECH] 2 : *the liquid used to remove exposed positive resist.* [SEMATECH]

Dielectric constant: *that property which determines the electrostatic energy stored per unit volume for unit potential gradient. The numerical value is usually given relative to a vacuum.* (Copyright 1993 IEEE. All rights reserved.)

Diffusion: *a high-temperature process in which desired chemicals (dopants) on a wafer are redistributed within the silicon to form a device component.* [SEMATECH]

Diffusion pump: *a vacuum pump that uses a stream of oil vapor to expel gases from the volume being evacuated and to create a high vacuum.* [SEMATECH]

Dopant: *in silicon technology, a chemical element incorporated in trace amounts in a semiconductor crystal or epitaxial layer to establish its conductivity type and resistivity.* [Adapted from SEMI M9-90 and M8-84]

Dopant density: *in an uncompensated extrinsic semiconductor, the number of dopant impurity atoms per unit volume, usually given in atoms/cm3, although the SI unit is atoms/m3. Symbols: N_D for donor impurities and N_A for acceptor impurities.* [ASTM F1241]

Dust: 1 : *a discrete particle of material on a wafer or reticle, usually removable by the solvent cleaning method.* [SEMATECH] 2: *in flat panel display substrates, a foreign particle that contaminates the glass surface.* [SEMI D9-94]

Edge bead: 1 : *a residual resist that remains on the edge of a substrate after the application process.* [SEMATECH] 2 : *a thin (3 mm) ring at the edge of the wafer in which photoresist is selectively removed by solvent or exposure.* [SEMATECH]

Electromagnetic interference (EMI): *any electrical signal in the nonionizing (suboptical) portion of the electromagnetic spectrum with the potential to cause an undesired response in electronic equipment.* [SEMI E33-94]

Electron beam lithography: *a direct-write lithography technique using a beam of electrons to expose resist on a wafer.* [SEMATECH]

Electrostatic discharge (ESD): 1 : *a sudden electric current flow, such as*

between a human body and a metal oxide semiconductor, with potential damage to the component. [SEMATECH] 2 : *the transfer of electrostatic charge between bodies at different electrostatic potentials.* [SEMI E33-94]

Ellipsometer: *equipment used to measure the thickness and refractive index of dielectric films.* [SEMATECH]

Epitaxial layer: *in semiconductor technology, a layer of a single crystal semiconducting material grown on a host substrate which determines its orientation.* [SEMI M2-94 and ASTM F1241]

Epitaxy (epi): *a silicon crystal layer grown on top of a silicon wafer that exhibits the same crystal structure orientation as the substrate wafer with a dissimilar doping type or concentration or both. Examples are p/p+, n/n+, n/p, and n/n.* [SEMATECH]

Etch: *a category of lithographic processes that remove material from selected areas of a die. Examples are nitride etch and oxide etch.* [SEMATECH] 2 *: in the manufacture of silicon wafers, a solution, a mixture of solutions, or a mixture of gases that attacks the surfaces of a film or substrate, removing material either selectively or nonselectively.* [SEMI M1-94 and ASTM F1241]

Etchant: *an acid or base (in either liquid or gaseous state) used to remove unprotected areas of a wafer layer. Examples are potassium hydroxide, buffered oxide etch, and sulfur hexafluoride.* [SEMATECH]

Evaporation: *an operation that uses heat and vacuum to remove a material from a source and deposit it on a surface. The deposition step of an evaporation operation is condensation.* [SEMATECH]

Evaporator: *a high-vacuum apparatus for evaporating materials.* [SEMATECH]

Fab: *the main manufacturing facility for processing semiconductor wafers.* [SEMATECH]

Fault: 1 : *an accidental condition that causes a functional unit to fail to perform its required function.* [SEMATECH] 2 : *a defect-causing out-of-spec operation of an integrated circuit.* [SEMATECH]

Feature size: 1 : *the physical dimensions of an individual pattern element, usually expressed as minimum feature size. For example, a 0.8 micrometer process has a minimum gate dimension of 0.8 micrometer.* 2 : *in surface characterization, any measurable three-dimensional surface irregularity, not necessarily oriented to any particular reference plane.* [SEMATECH]

Flat: *on a semiconductor wafer, a portion of the periphery of a circular wafer that has been removed to a chord.* [SEMI M1-94 and ASTM F1241]

Focal plane: *the plane perpendicular to the optical axis of an imaging system that contains the focal point of the imaging system.* [SEMI M1-94]

Four-point probe: *an electrical probe arrangement for determining the resistivity of a material, in which separate pairs of contacts are used (1) for passing current through the specimen and (2) for measuring the potential drop caused by the current.* [SEMI M1-94 and ASTM F1241] *Also called collinear four-probe array.*

Front end-of-line (FEOL): *all processes from wafer start through final contact window processing.* [SEMATECH]

G line: *exposure wavelength of 436 nanometers.* [SEMATECH]

Gate oxide: *a thin, high-quality silicon dioxide film that separates the gate electrode of a metal oxide semiconductor transistor from the electrically conducting channel in the silicon.* [SEMATECH]

HAM – horizontal alignment mark: *image located on right and left side of field used by stepper for local alignment.*

Hard bake: *heat treatment of a wafer after develop to fully harden the resist prior to etch.* [SEMATECH]

Hexamethyldisilazane (HMDS): *a chemical compound used as a preresist wafer treatment to improve adhesion of resist to wafers.* [SEMATECH]

High-efficiency particulate air (HEPA) filter: *a replaceable extended media, dry-type filter in a rigid frame and having a minimum particle-collection efficiency of 99.97% on all particles larger than 0.3 micrometer.* [SEMATECH]

Horizontal furnace: *a family of furnaces in which the wafers are loaded and processed in a horizontal tube.* [SEMATECH]

HPP – hot point probe: *doping type characterization tool, can be used to determine oxide etch completeness.*

Hydrofluoric acid (HF): *a poisonous solution of hydrogen fluoride gas in water. This colorless, fuming liquid is extremely corrosive and will etch glass. Hydrofluoric acid is used to etch silicon dioxide and, when combined with other acids, silicon.* [SEMATECH]

Hydrogen (H_2): *the lightest known gas; hydrogen vapors are highly flammable, colorless, odorless, tasteless, and nontoxic. Hydrogen is used as a means of providing a reducing atmosphere, as a carrier gas for epitaxial processes, and as a reagent to produce high-purity water. It sometimes is used in gas mixtures of fluorine-based plasma etchant for the processing of silicon dioxide film.* [SEMI C3.4-88]

Hydrogen peroxide (H_2O_2): 1 : *a colorless, unstable compound, soluble in water and alcohol.* [SEMI C1.9-90] 2 : *a compound used as a catalyst in many etch formulations, such as piranha.* [SEMATECH]

I line: *exposure wavelength of 365 nm.* [SEMATECH]

Index of refraction: *the relative index of refraction defined by Snell's law as the ration of the sine of the angle of incidence to the sine of the angle of refraction.* [ASTM F1241]

Inert gas: *a gas that, at ambient conditions, does not react chemically with other materials.* [SEMI S4-92]

Initial oxide: *the first silicon oxide layer grown on the surface of a silicon wafer before the first pattern step.* [SEMATECH]

Inorganic: *describes materials that do not contain carbon.* [SEMATECH]

Integrated circuit (IC): 1 : *two or more interconnected circuit elements on a single die.* [SEMATECH] 2 : *a fabrication technology that combines most of the components of a circuit on a single-crystal silicon wafer.* [SEMI Materials, Vol. 3, Definitions for Semiconductor Materials]

Interconnect: 1 : *a highly conductive material, usually aluminum or polysilicon, that carries electrical signals to different parts of a die.* [SEMATECH] 2 : *the wiring between elements on a die, package, or board.* [1994 National Technology Roadmap for Semiconductors]

Interstitial: *in a crystalline solid, an atom that is not located on a lattice site.* [SEMATECH]

Junction spiking: *the penetration of a junction by aluminum, which occurs when silicon near the junction dissolves in aluminum and migrates along the interconnect lines. Aluminum then replaces silicon at the junction.* [SEMATECH]

Large scale integration (LSI): *the placement of between 100 and 1000 active devices on a single die.* [SEMATECH]

Lateral diffusion: *diffusion parallel to the wafer surface. Lateral diffusion of metal-oxide semiconductor source/drain*

regions determines the effective channel length of the device. [SEMATECH]

LCR meter – Inductance, capacitance, resistance meter: *electrical characterization instrument used to determine capacitance and inductance of devices.*

Linewidth: 1 *: in semiconductor technology, the distance between the air-line material boundaries at some specified height above the interface between the patterned layer in which the line is formed and the underlying layer.* [SEMI P19-92] 2 : *a measurement with which to determine critical dimensions.* [SEMATECH]

Linewidth, etched: *a measurement of the etched feature produced on a wafer by transfer of the resist pattern into the wafer.* [SEMATECH] *Also called final inspect (F/I) and post etch.*

Linewidth, PR: *a measurement of the resist feature produced on a wafer during photo processing after the develop process.* [SEMATECH] *Also called develop/inspect (D/I) and pre-etch.*

Lithography: *a process in which a masked pattern is projected onto a photosensitive coating that covers a substrate.* [SEMATECH] *Also called photolithography.*

Majority carrier: *a type of charge carrier constituting more than one-half the total charge carrier concentration (for example, holes in p-type material).* [SEMI M1-94 and ASTM F1241]

Mask: 1 : *a flat, transparent plate that contains the photographic image of wafer patterns necessary to define one process layer.* [SEMATECH]
2 : *a selective barrier to the passage of radiation or matter.* [ASTM F127-84] *Also called etched metal mask or any specific mask type. Contrast photomask.*

Mask level: *a numbered mask in a sequence that includes device patterns, test patterns, and alignment patterns.* [SEMATECH]

Mass flow controller (MFC): *a self-contained device (consisting of a transducer, control valve, and control and signal-processing electronics) commonly used in the semiconductor industry to measure and regulate the mass flow of gas.* [SEMI E29-93]

Material safety data sheet (MSDS): 1 : *written or printed material concerning a hazardous material that is prepared in accordance with the provisions of 29 CFR 1910.1200. (See UFC "88" 9.115.) (Form OSHA 20)* [SEMI S2-91] 2 : *the descriptive data provided on a data sheet recommended by the Occupational Safety and Health Administration (OSHA) to provide information regarding the hazards of materials to prevent and respond to emergency situations.* [SEMATECH]

Medium scale integration (MSI): *the placement of between 10 and 100 active devices on a single die.* [SEMATECH]

Metallization: *the deposition of a thin film of conductive metal onto a wafer or substrate by use of either chemical or physical vapor deposition (for example, sputtering).* [SEMATECH]

Micrometer (µm): *a metric unit of linear measure that equals 1/1,000,000 meter (10^{-6} m), or 10,000 angstroms. The diameter of a human hair is approximately 75 micrometers.* [SEMATECH] *Also called micron.*

Minority carrier: *a type of charge carrier constituting less than one-half of the total charge -carrier concentration (for example, electrons in p-type material).* [SEMI M1-94 and ASTM F1241] *Contrast majority carrier.*

Misalignment: *a process defect in which a pattern layer does not overlay properly with previous layers.* [SEMATECH]

Nanometer (nm): *one billionth (10^{-9}) of a meter; used in the measurement of the wavelength of light.* [SEMATECH]

Nitric acid (HNO_3): *a strong, colorless or yellowish liquid oxidant that is highly corrosive and a potential fire hazard. This acid is prepared by the action of sulfuric acid on nitrates and by the oxidation of ammonia. Nitric acid is used to clean silicon wafers and etch metals.* [SEMI C1.12-90]

Nitrogen (N_2): *normally a diatomic gas, but also a cryogenic liquid (a liquid at low temperature). Its vapors are odorless, tasteless, and nonflammable. Nitrogen is used in purging, blanketing, pressurizing systems, and cooling systems. It also is used as a carrier gas in chemical vapor deposition and at ambient temperature for sintering and annealing.* [SEMI C3.5-88]

OAT – optical alignment target: *image located on wafer used by stepper for global alignment.*

Orientation: *of a single crystal surface, the crystallographic plane, described in terms of its Miller indices, with which the surface is ideally coincident. NOTE-In semiconductor single crystals, where the surface of a wafer cut from the crystal usually corresponds closely (within a degree or several degrees) to a low index plane, such as a {100} or {111} plane, the surface orientation is frequently described in terms of the maximum angular deviation of the mechanically prepared surface from the low index crystallographic plane.* [ASTM F1241]

Overlay (OVL): 1 : *the precision with which successive masks can be aligned with previous patterns on a silicon wafer.* [1994 National Technology Roadmap for Semiconductors] 2 : *in semiconductor wafers and flat panel display substrates, a vector quantity defined at every point on the wafer or substrate. It is the difference, O, between the vector position, p_1, of a substrate geometry, and the vector position of the corresponding point, p_2, in an overlaying pattern, which may consist of photoresist.* [Adapted from SEMI P18-92 and D8-94]

Overlay accuracy: *relative deviation of pattern position between two masks.* [SEMI P21-92]

Oxidation: *a high-temperature chemical reaction in which the silicon of the wafer surface reacts with oxygen or water vapor to form an oxide such as silicon dioxide, typically at temperatures greater than 800 degrees C.* [SEMATECH]

Oxide (Ox): *a dielectric, or nonconducting film, grown or deposited on the surface of a wafer.* [SEMATECH]

Oxide etch: *an etch process in which unprotected areas of the oxide layer are eroded by use of a chemical to expose the underlying layer.* [SEMATECH]

Oxygen (O_2): *a colorless, odorless, nontoxic, and oxidizing gas that supports combustion. Oxygen is used in the chemical vapor deposition of silicon dioxide, as a source for oxidation, as a reactant to produce high-purity water, and in plasma etching and stripping.* [SEMI C3.22-88]

Particle: 1 : *a minute quantity of solid or liquid matter.* [SEMATECH] *Also see dirt.* 2 *: in the manufacture of photolithographic pellicles, material that can be distinguished from the film, whether on the film surface or embedded in the film.* [SEMI P5-94]

Particulate: 1 : *discrete particle of dirt or other material.* [ASTM F1241] *Also see dirt.* 2 (dust) : *discrete particle of material that can usually be removed by (nonetching) cleaning.* [SEMI M10-89] 3 : *describes material in small, discrete pieces; anything that is not a fiber and has an aspect ratio of less than 3 to 1. Examples are dusts, fumes, smokes, mists, and fogs.* [SEMATECH]

Pattern, test: *an image that appears on a photomask for registration or evaluation.* [ASTM F127-84]

Photomask, negative: *a photomask having an opaque background and transparent images.* [ASTM F127-84]

Photomask, positive: *a photomask having transparent background and opaque images.* [ASTM F127-84]

Photoresist (PR): *a radiation-sensitive material that, when properly applied to a variety of substrates and then properly exposed and developed, masks portions of the substrate with a high degree of integrity.* [ASTM F127-84]

Piranha: *a reactive etch solution composed of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) to remove organic contaminants from a silicon wafer or a film such as SiO_2.* [SEMATECH]

Pitch: *the distance between a point on an image and a point on the corresponding image in an adjacent functional pattern that lies in either a row or column on a photomask or reticle.* [SEMATECH]

P_2O_5 – phosphorus pentoxide: *volatile oxide used to transfer phosphorus to the wafer.*

Polycrystalline silicon (poly): *a nonporous form of silicon made up of randomly oriented crystallites or domains, including glassy or amorphous silicon layers.* [ASTM F399-88] *Also called poly and polysilicon.*

Post-exposure bake (PEB): *a bake after expose and prior to develop to diffuse the photoactive component of the resist; minimizes standing waves and ensures a clean develop.* [SEMATECH]

Primary orientation flat: *the flat of longest length on the wafer, oriented such that the chord is parallel with a specified low index crystal plane.* [ASTM F1241] *Also called major flat.*

Prober: *a piece of hardware that allows a collection of probes to be brought into contact with the die on a wafer for the purpose of testing an integrated circuit.* [1994 National Technology Roadmap for Semiconductors]

Profilometer: 1 : *an instrument for measuring the topographical profile of a surface.* [SEMI M1-94 and ASTM F1241] 2 : *An instrument for measuring the roughness of a surface by means of a diamond-pointed stylus attached to a coil in an electric field; movement of the stylus across the surface induces a current proportional to the surface roughness.* [SEMATECH]

PSG – phosphosilicate glass: *silicon dioxide containing a high concentration of phosphorus. Forms when P_2O_5 reacts with silicon at high temperature.*

Pure water: *water suitable for use in semiconductor processing because of the very small level of impurities. Resistivity in pure water is high because the conductive impurities are at a low level.* [SEMATECH]

Pyrogenic steam: *water vapor generated by combining hydrogen and oxygen in the furnace working chamber to produce high purity steam.* [ASTM F1241]

Quartz carrier: *a supporting structure that holds substrates during high-temperature operation.* [SEMATECH] *Also called boat.*

Quartzware: *containers made from amorphous material, which is resistant to high temperature. Examples are the furnace tube and the quartz carrier.* [SEMATECH]

Relative humidity (RH): *the quantity of water vapor present in the atmosphere as a percentage of the quantity that would saturate at the existing temperature.* [SEMATECH]

Resistivity (ρ): 1 : *of a semiconductor, the ratio of the potential gradient parallel with the current in the material to the current density. Units are Ω-cm .* [SEMI M4-88] 2 : *the resistance that a unit volume of semiconductor material offers to the passage of electricity when the electric current is perpendicular to two parallel faces.* [SEMI M1-94] 3 (electrical) : *the measure of difficulty with which charge carriers flow through a material. Resistivity is the reciprocal of conductivity. DISCUSSION-The resistivity of a semiconductor or other material is the ratio of the potential gradient (electronic field) parallel with the current to the current density.* [ASTM F1241]

Resist lifting: *on a wafer, the loss of adhesion of a resist coating to its substrate.* [SEMI P3-90] *Also called photo lifting.*

Resolution: *the fineness of detail revealed by an optical device. Resolution is usually specified as the minimum distance by which two lines in the object must be separated before they can be revealed as separate lines in the image.* [ASTM E7-90]

Reticle: *a very flat glass plate that contains the patterns to be reproduced on a wafer; the image may be equal to or larger than the final projected image. Typical reticle substrate material is quartz, and typical magnifications are 10, 5, and 1 times final size. The reticle is used in a stepper.* [SEMATECH]

Reverse osmosis (RO): *a technique used in desalination treatment. Pressure is applied to the saline solution, forcing pure water to pass from the solution through a membrane that will not pass the undesired ions.* [SEMATECH]

Schottky barrier diodes: *a semiconductor diode that is formed by contact between a semiconductor layer and a metal coating; it has a nonlinear rectifying characteristic. Hot carriers are emitted from the metal coating that is the diode base; since majority carriers predominate, there is essentially no injection or storage of minority carriers to limit switching speeds. Also known as a hot-carrier diode.* [SEMATECH]

Secondary flat: *a flat of length shorter than the primary orientation flat, whose position with respect to the primary orientation flat identifies the type and orientation of the wafer. DISCUSSION-In some cases, one or more nonstandard "secondary" flats are specified to identify other attributes of the wafer.* [ASTM F1241] *Also called minor flat.*

Sheet resistance (R_s) (Ω or Ω per square): *of a semiconductor or thin metal film, the ratio of the potential gradient (electric field) parallel with the current to the product of the current density and thickness.* [ASTM F1241]

Single crystal silicon: *an arrangement of atoms in a solid that has perfect periodicity (that is, no defects).* [SEMATECH]

Si:P_2O_7 – silicon pyrophosphate: *stable solid source used for predeposition of phosphorus. During predeposition Si:P_2O_7 decomposes to a volatile compound to transfer phosphorus to the wafer.*

Small scale integration (SSI): *the placement of between 2 and 10 active devices on a single die.* [SEMATECH]

Solvent: *a substance capable of dissolving another substance, or substances, to form a solution. Examples are isopropyl alcohol, methyl alcohol, and xylene.* [SEMATECH]

Solvent residue: 1 : *a type of dirt found on wafer surfaces after solvent evaporation from the surface. The residue either is left by the solvent itself or is material that the solvent has removed from the surface and redeposited.* [ASTM F1241] 2 : *type of film found on wafer surfaces after solvent evaporation from the surface.* [SEMI M10-89]

SPA – semiconductor parameter analyzer: *electrical characterization instrument with multiple current/voltage sources and sweeps. Used to determine I-V characteristics of devices.*

Spin: *an operation in which a metered amount of resist is applied to a wafer while it is spinning; the operation in which a substrate is rotated about an axis perpendicular to its surface while, or immediately after, a coating material is applied in liquid form to the substrate surface.* [SEMATECH]

Step and repeat: *an operation that, by the use of a stepper, repeats the image over the wafer as the stage makes small steps in the X and Y axes. The operation dimensionally positions multiples of the same or intermixed functional patterns on a given area of a photoplate or a film by repetitions, contact printing, or projection printing of a single original pattern of each type.* [SEMATECH]

Step coverage: *the ratio of thickness of film along the walls of a step to the thickness of the film at the bottom of a step. Good step coverage reduces electromigration and high-resistance pathways.* [SEMATECH]

Stepper: *equipment used to transfer a reticle pattern onto a wafer.* [SEMATECH]

Stripper: *a chemical solvent used to remove resist film from wafers.* [SEMATECH]

Stripping: *an operation that completely removes a resist coating.* [SEMATECH]

Sulfuric acid (H_2SO_4): *a strong, poisonous, corrosive liquid that will mix with water and that will dissolve most metals. Sulfuric acid is used to clean wafers and to remove resist.* [SEMI C1.16-90]

Throughput: *the number of wafers per hour through a machine, assuming 100% equipment uptime and a fully loaded machine. The number is adjusted downward for any detracting factors one wants to consider (for example, downtime, setup time, idle time, etc.)* [SEMATECH]

Torr: *unit of measure for the pressure exerted by 1 mm of mercury, equal to 1/760th of standard atmospheric pressure; used to measure pressure in vacuum systems. The corresponding SI unit is the pascal (Pa).* [SEMATECH]

Trapped charges: *charges trapped either in the gate oxide or, in the case of a lightly doped drain (LDD) metal-oxide semiconductor field-effect transistor (MOSFET), in the spacer region. Trapped charges in the gate or the spacer lead to threshold voltage shift or to transconductance degradation, respectively.* [SEMATECH]

Ultrapure water (UPW): *deionized and filtered water.* [SEMATECH]

Undercutting: *the lateral etching into a substrate under a resistant coating, as at the edge of a resist image.* [ASTM F127-84]

UV – ultraviolet light: *invisible short-wavelength light used for exposing PR coated wafers in photolithography.*

Vacuum: *an absence of air or other gas.* [SEMATECH]

Very large scale integration (VLSI): *the placement of between 1,000 and 1,000,000 components on a die.* [SEMATECH]

Wafer: *in semiconductor technology, a thin slice with parallel faces cut from a semiconductor crystal.* [ASTM F1241] *Also called a slice.*

Wafer carrier: 1 : *any vessel or supporting structure used to contain or transfer wafers during processing.* [SEMATECH] 2 : *a device for holding a wafer for various processing steps in semiconductor manufacturing.* [SEMI E1-86]

Wafer, dummy: *a noncritical wafer added to a load-sensitive operation or run to complete a load of the equipment or process. Dummy wafers are never measured.* [SEMATECH] *Also called filler wafer.*

Wafer flat: *straight cuts on the side of a wafer; used to indicate the type of free-carrier conduction and orientation of the crystal surface. Also used to align the wafer during processing and scribing.* [SEMATECH]

Wet chemical etch: *a physical etch process that uses chemicals such as hydrofluoric acid to remove unprotected areas of a wafer layer.* [SEMATECH]

Resistivity

$\sigma = q(\mu_n n + \mu_p p)$

$\rho = \frac{1}{d}$

$n \approx N_d$ if $n >> p$ — intentiona l n - type doping

$\rho \approx \frac{1}{q\mu_n N_d}$ — $\mu_n = f(N_d)$ not a constant

$N_d = f(\rho)$ — GT – 1

Four Point Probe

$\rho_0 = 2\pi s \frac{V}{I}$ — s = spacing, ∞ thickness

$\rho = a\rho_0$ — thickness correction, GT - 2

$\rho = 4.53t \frac{V}{I}$ — only if t/s < 0.5

Sheet Resistance

$R_s = \frac{\rho}{t}$

$R_s = 4.53 \frac{V}{I}$ — only if $\frac{t}{s} < 0.5$

$R_s = C \frac{V}{I}$ — if $\frac{d}{s} < 40$, GT – 3

Chemistry of Phases

$P + F = C + 2$ — phase rule

$x = \frac{w_B}{(w_A + w_B)}$ — compositio n

$w_S(x_S - x_i) = w_L(x_i - x_L)$ — lever rule

Diffusion

$F = -D \frac{\partial N(x,t)}{\partial x}$ — Fick's first law

$D = D_\infty e^{-E_0/kT}$ — diffusion coefficien t

$\frac{\partial N}{\partial t} = D \frac{\partial^2 N}{\partial x^2}$ — Fick's second law

Predep

constant source=predep=erfc

$N(x,t) = N_0 \operatorname{erfc} \frac{x}{\sqrt{4Dt}}$ — GT - 13

N_0 = solid solubility

$Q = \int F(0)dt = 2N_0 \sqrt{\frac{Dt}{\pi}}$ — Dose

$N_{01} \operatorname{erfc} \frac{x}{\sqrt{4D_1 t}} = N_C \operatorname{erf} \frac{x}{\sqrt{4D_0 t}}$ predep junction

Drive

limited source=drive=Gaussian

$N(x, t_1, t_2) = \frac{2N_{01}}{\pi} I(\alpha, \beta)$ exact solution, $I(\alpha,\beta)$ tabulated

$\alpha = \sqrt{\frac{D_1 t_1}{D_2 t_2}}$

$\beta = \frac{x^2}{4(D_1 t_1 + D_2 t_2)}$

$N_{02} = \frac{2N_{01}}{\pi} \tan^{-1}\alpha$

$\Delta = Dt$ — shorter notation

$N(x, t_2) = N_{02} e^{\frac{-x^2}{4\Delta_2}}$ approximat e solution

$N_{02} = \frac{2N_{01}}{\pi} \sqrt{\frac{\Delta_1}{\Delta_2}}$

$\Delta_* = \frac{\Delta_1}{1.3} + \Delta_2$ S & M approximat ion

$\Delta_* = \frac{\Delta_1}{1.3} + \int D(t)dt$ time dependent diffusion

ransistor Equations

$N_e(x) = N_{0e} \operatorname{erfc} \frac{x}{\sqrt{4\Delta_e}}$ — Emitter

$N_b(x) = N_{0b} e^{\frac{-x^2}{4\Delta_{b*}}}$ — Base $\Delta_{b*} = \Delta_{b1} + \Delta_{b2} + \Delta_{b3}$

$N_c(x) = N_c \operatorname{erf} \frac{x}{\sqrt{4\Delta_c}}$ — Collector $\Delta_c = \Delta_{c1} + \Delta_{c2} + \Delta_{c3}$

$N_e(x_{je}) = N_b(x_{je}) = N_{b'}$ — Emitter – base junction

$N_b(x_{jc}) = N_c$ — Collector – base junction (SOA)

Irvin Curves

Diffused Layer sheet resistance

$\bar{\sigma} = \frac{q}{x_j - x_0} \int_{x_0}^{x_j} \mu_m [N(x) - N_c] dx$ Average conductivi ty

$N_s = N(x_0)$

$R(\Omega/sq) = \frac{1}{x\bar{\sigma}(x_j - x_0)}$

$x_0 = 0$ and $N_s = N_{0e}$ — for R_{se}

$x_0 = x_{jc}$ and $N_s = N_{0b}$ — for R_{bb}

$x_0 = 0$ and $N_s = N_{0b}$ — for R_{sb}

Ion Implantation

$ZQA = \int I(t)dt$ — Q = dose

$N(x) = N_p e^{\frac{-1}{2}\left(\frac{x - R_p}{\Delta R_p}\right)^2}$

$N_p = \frac{Q}{\sqrt{2\pi}\Delta R_p}$

Junction Capacitance

$C = \frac{\varepsilon A}{w}$

$\varepsilon = \varepsilon_s \varepsilon_0$

$w(V) = \sqrt{\frac{2\varepsilon(V_0 - V)}{qN_d}}$

Breakdown

$I_{sat} = qA \frac{D_p p_n}{L_p} + qA \frac{D_n n_p}{L_n}$

$M = \frac{n_0}{n_{in}} = \frac{1}{1 - P}$

$P = \int \alpha_i(x)dx$

$A = \left| \frac{\partial N(x,t)}{\partial x} \right|_{x_j}$

MOS Energy Bands

$\varphi_f = E_f - E_i = kT \ln\left(\frac{N_d}{n_i}\right)$ — Fermi level

$\varphi_s = 2\varphi_f$ — strong inversion

$w_{max} = \sqrt{\frac{2\varepsilon(2\varphi_f)}{qN_d}}$

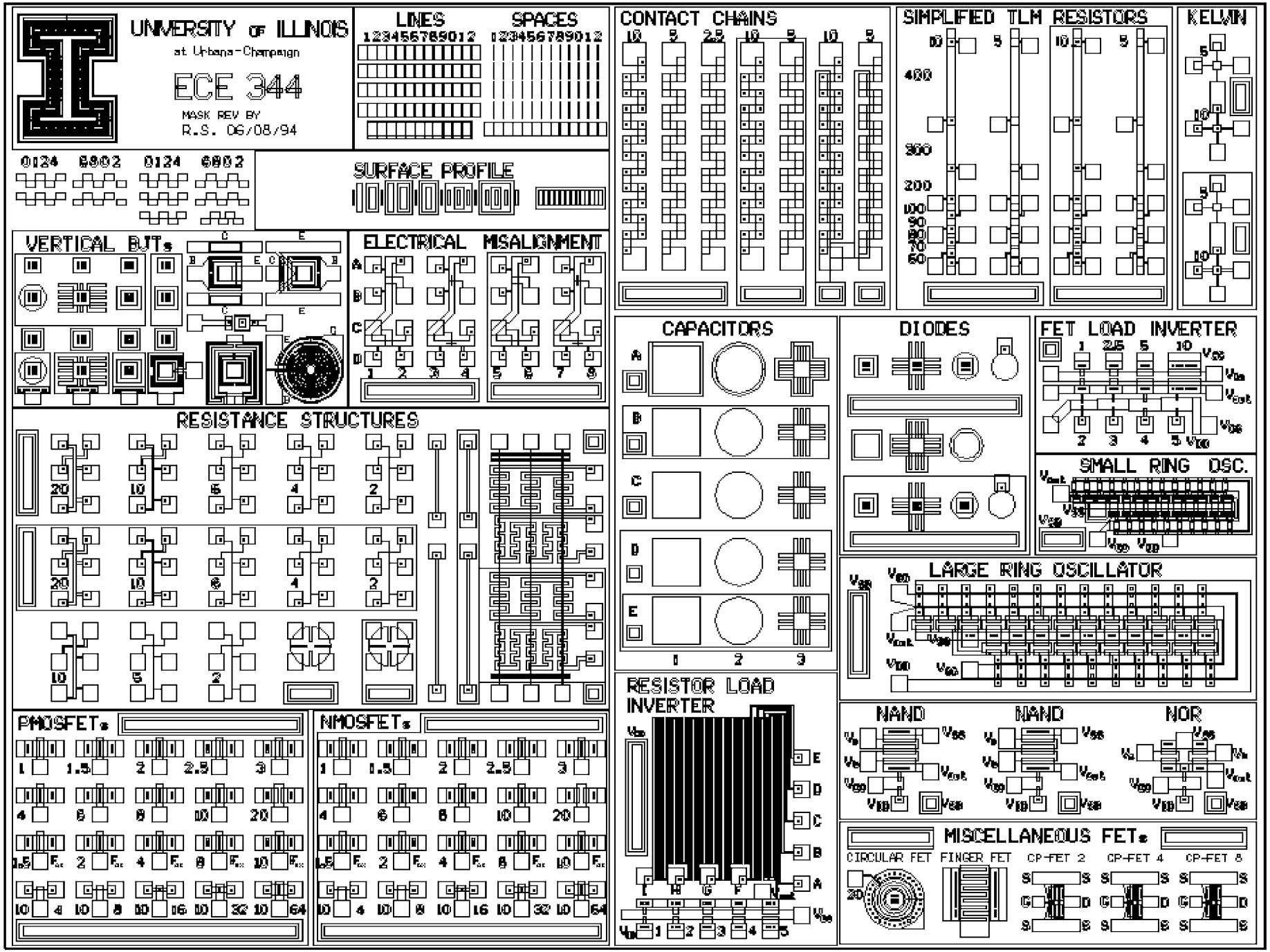
$\varphi_{ms} = \varphi_m - \varphi_s$

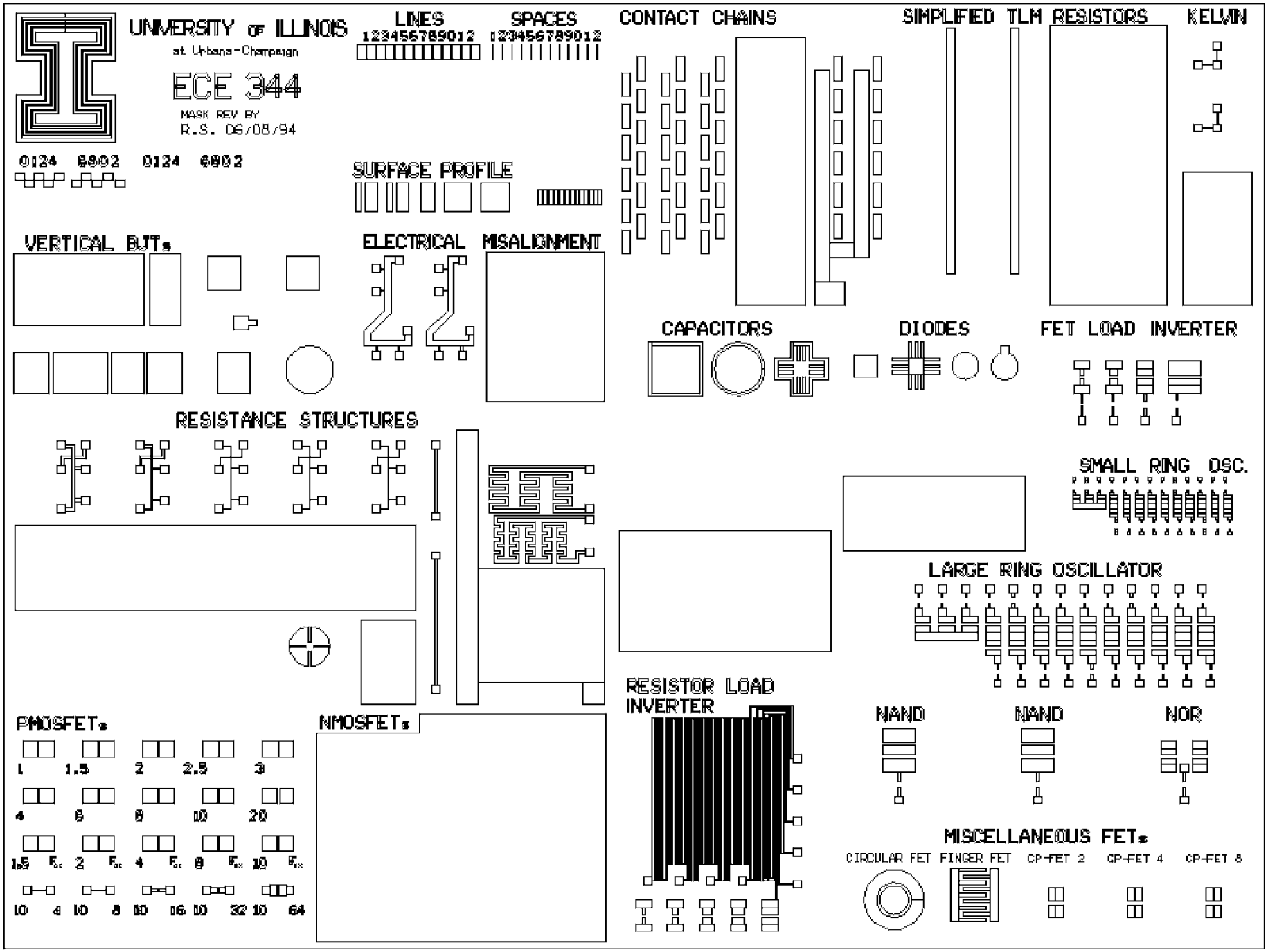
$Q_{ss} = qN_{ss}$

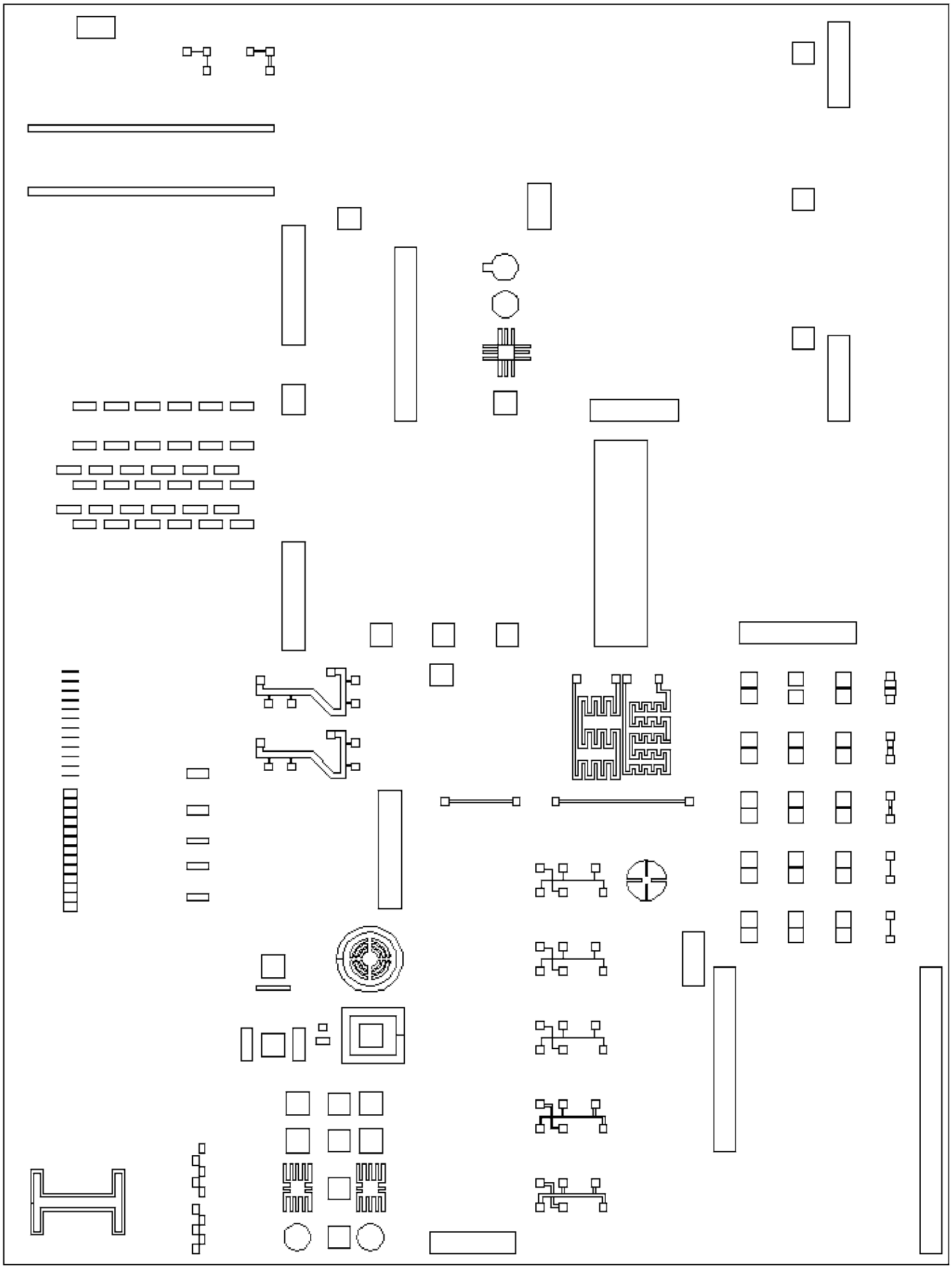
$Q_s = \pm qN_b w_{max}$ — ionized donors are +charge; ionized acceptors are – charge

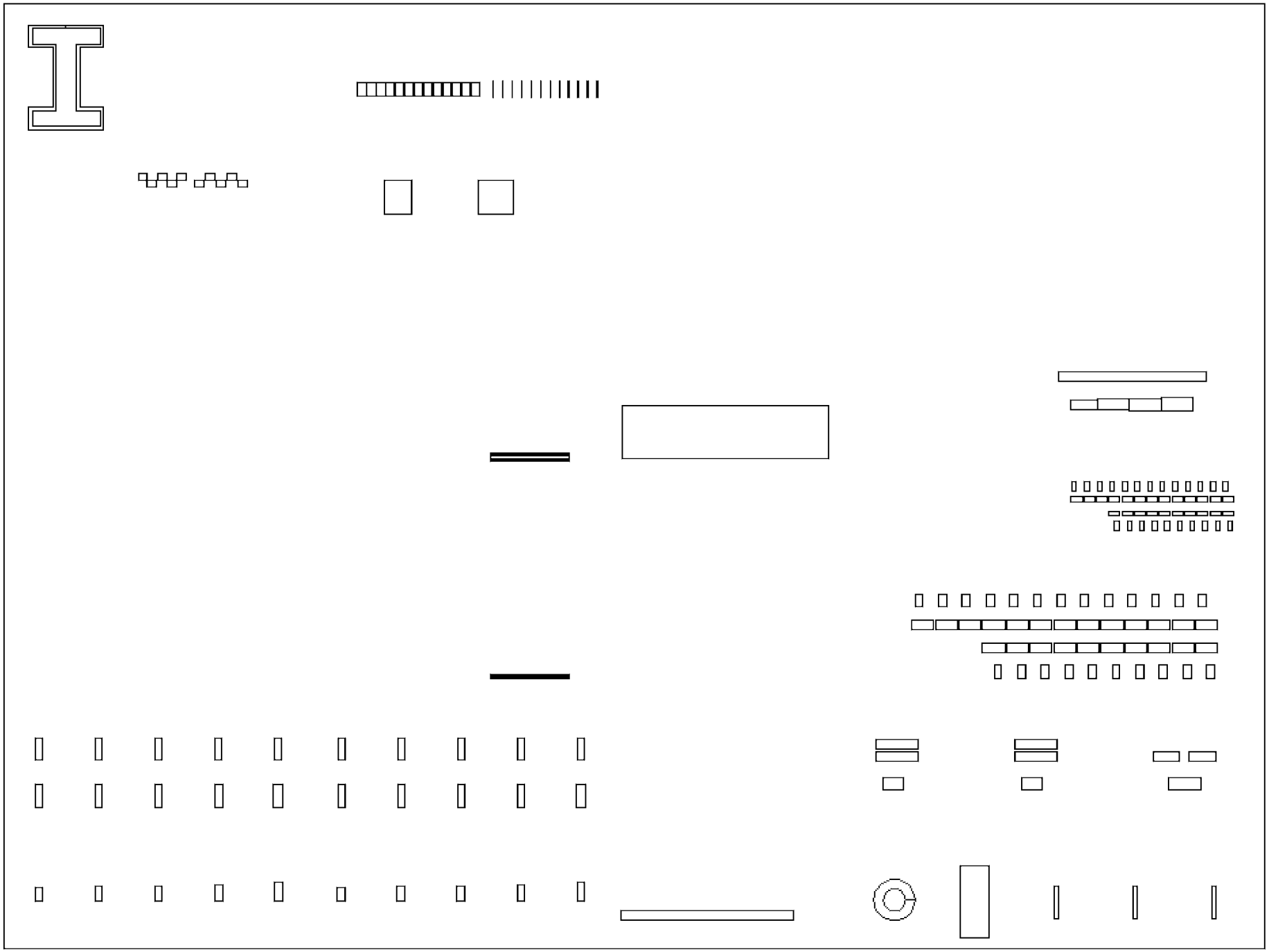
$c_i = \frac{\varepsilon_i}{t}$

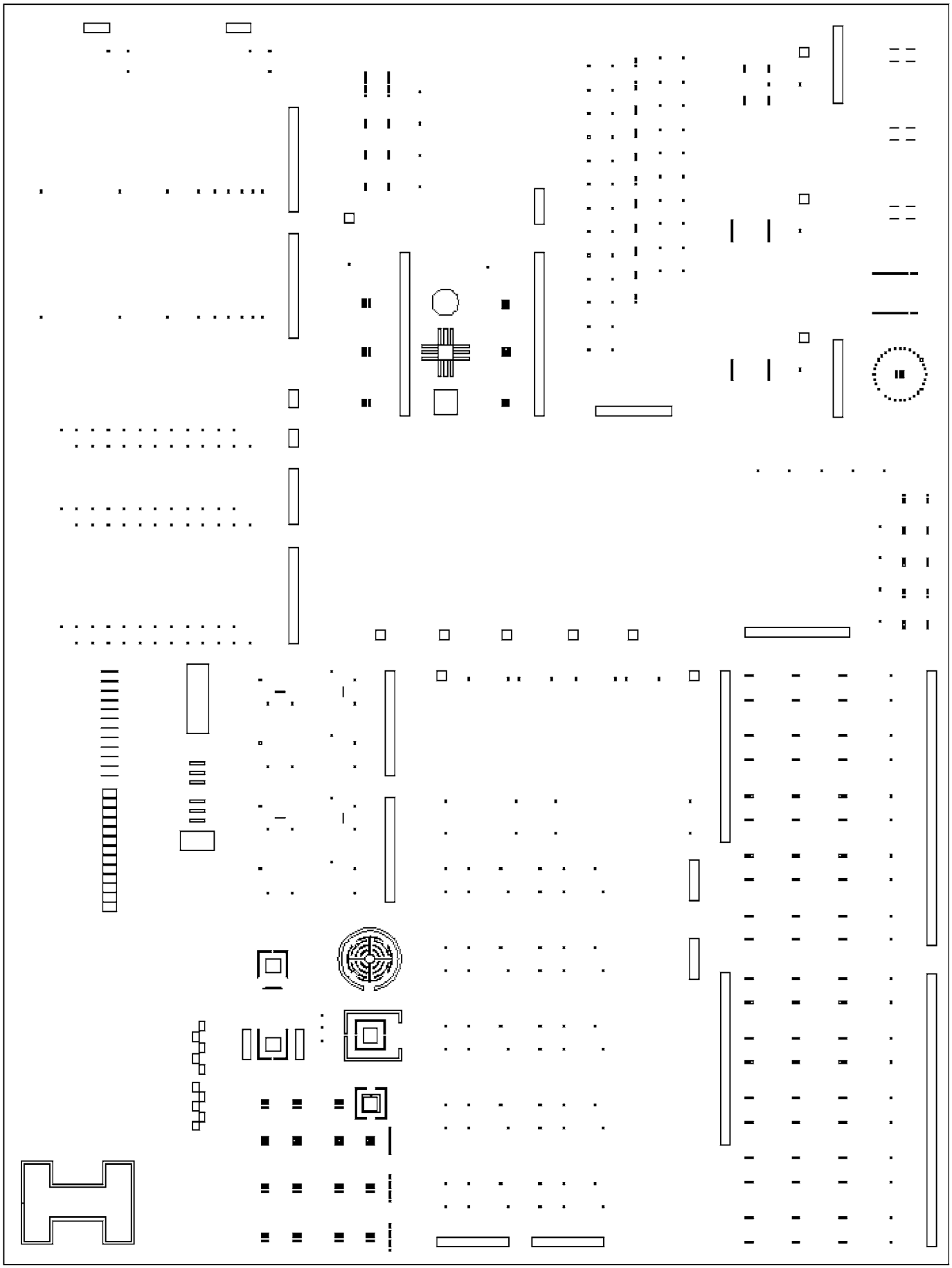
$V_T = \varphi_{ms} - \frac{Q_{ss}}{c_i} - \frac{Q_s}{c_i} \pm 2\varphi_f$ — + for p – substrate; – for n – substrate

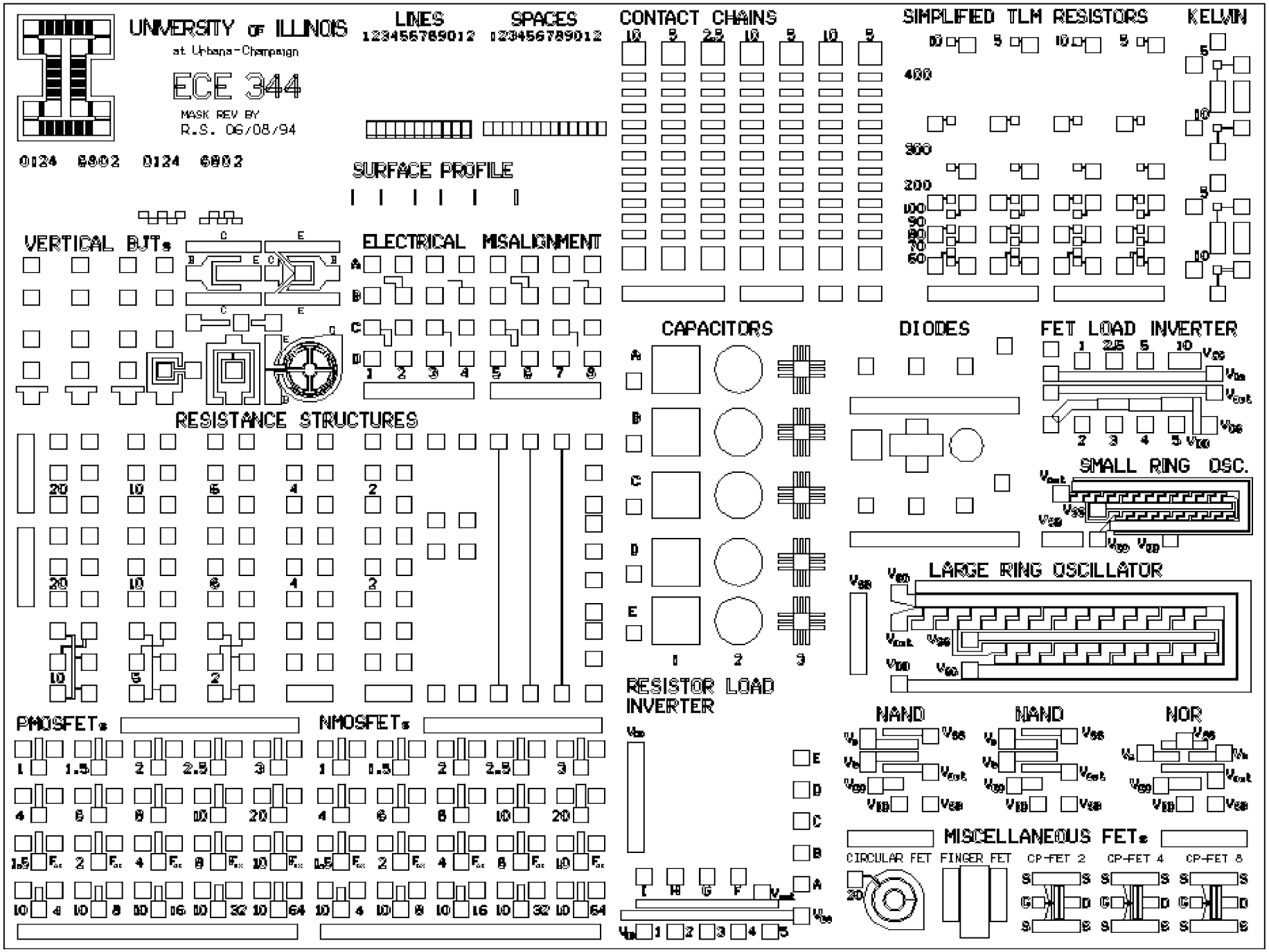

UNIVERSITY OF ILLINOIS
at Urbana-Champaign
ECE 344
MASK REV BY
R.S. 06/08/94
LINES
SPACES
CONTACT CHAINS
SIMPLIFIED TLM RESISTORS
KELVIN
SURFACE PROFILE
VERTICAL BJTs
ELECTRICAL MISALIGNMENT
CAPACITORS
DIODES
FET LOAD INVERTER
SMALL RING OSC.
RESISTANCE STRUCTURES
LARGE RING OSCILLATOR
RESISTOR LOAD INVERTER
NAND
NAND
NOR
PMOSFETs
NMOSFETs
MISCELLANEOUS FETs
CIRCULAR FET
FINGER FET
CP-FET 2
CP-FET 4
CP-FET 8

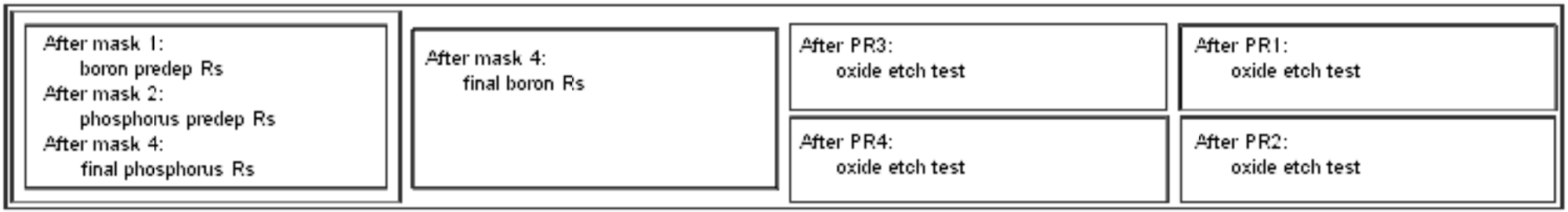

UNIVERSITY OF ILLINOIS
at Urbana-Champaign
ECE 344
MASK REV BY
R.S. 06/08/94
LINES
123456789012
SPACES
123456789012
0124 6802 0124 6802
SURFACE PROFILE
CONTACT CHAINS
SIMPLIFIED TLM RESISTORS
KELVIN
VERTICAL BJTs
ELECTRICAL MISALIGNMENT
CAPACITORS
DIODES
FET LOAD INVERTER
RESISTANCE STRUCTURES
SMALL RING OSC.
LARGE RING OSCILLATOR
RESISTOR LOAD INVERTER
NAND
NAND
NOR
PMOSFETs
1 1.5 2 2.5 3
4 6 8 10 20
1.5 F.C. 2 F.C. 4 F.C. 8 F.C. 10 F.C.
10 4 10 8 10 16 10 32 10 64
NMOSFETs
MISCELLANEOUS FETs
CIRCULAR FET
FINGER FET
CP-FET 2
CP-FET 4
CP-FET 8








UNIVERSITY OF ILLINOIS
at Urbana-Champaign
ECE 344
MASK REV BY
R.S. 06/08/94
0124 6802 0124 6802
LINES
123456789012
SPACES
123456789012
SURFACE PROFILE
CONTACT CHAINS
SIMPLIFIED TLM RESISTORS
KELVIN
VERTICAL BJTs
ELECTRICAL MISALIGNMENT
RESISTANCE STRUCTURES
CAPACITORS
DIODES
FET LOAD INVERTER
SMALL RING OSC.
LARGE RING OSCILLATOR
RESISTOR LOAD INVERTER
NAND
NAND
NOR
PMOSFETs
NMOSFETs
MISCELLANEOUS FETs
CIRCULAR FET
FINGER FET
CP-FET 2
CP-FET 4
CP-FET 8


After mask 1:
boron predep Rs
After mask 2:
phosphorus predep Rs
After mask 4:
final phosphorus Rs
After mask 4:
final boron Rs
After PR3:
oxide etch test
After PR4:
oxide etch test
After PR1:
oxide etch test
After PR2:
oxide etch test