

## **ECE 444**

### **Theory and Fabrication of Integrated Circuit Devices**

#### Course Goals

This is a senior elective laboratory course for electrical engineering and computer engineering majors. Students from other departments are also welcome, particularly those in Mechanical Engineering, Chemical Engineering, Materials Science and Engineering, and Physics. Graduate credit is available. The goals of this course are to provide a detailed understanding and hands-on laboratory experience in the wide range of technical processes that comprise modern integrated circuits. The course is intended to (a) be the primary core course for students seeking to pursue a career in integrated circuit fabrication, and (b) provide detailed background material for students interested in other aspects of the semiconductor industry, such as VLSI design or microprocessor architecture.

#### Instructional Objectives

By the time of Exam 1 (after 7 lectures) the students should be able to do the following:

1. Outline and describe the process flow diagram for the fabrication of MOS or bipolar integrated circuits (ICs). (a)
2. Draw the cross section and identify the final device that results from a given IC mask set, or design a set of masks that could be used to produce a given cross section. (c)

By the time of Exam 2 (after 14 lectures) the students should be able to do the following:

3. Explain the process and operation of advanced integrated bipolar and CMOS devices (a, c)
4. Explain the process for manufacturing silicon IC wafers from raw quartzite. (e)
5. Calculate the impurity doping density of a silicon wafer or epitaxial layer from four point probe measurements of the sheet resistance. (e)

By the time of Exam 3 (after 22 lectures) the students should be able to do the following:

6. Derive Fick's Laws for diffusion and explain the significance of the exponential form of the diffusion coefficient. (a)
7. Understand and explain Grove's model for oxidation, including the boundary layer, mass transfer coefficient, diffusion through an existing oxide layer, and reaction at the Si-SiO<sub>2</sub> interface. (a)
8. Define the oxide growth rate in the limits of thin and thick oxide layers. (c)
9. Design the process for a desired total oxide thickness using a combination of multiple dry or wet oxidation process steps. (c)
10. Understand the chemistry of photoresists and explain the differences, particularly in development, between positive and negative resists. (c)
11. Describe the complete optical system of several important photoimaging systems, such as the step-and-repeat projection aligner. (c)
12. Explain the advantages of electron beam lithography for design, development, and manufacturing. (c)

By the time of Exam 4 (after 28 lectures) the students should be able to do the following:

13. Understand the chemical process for wet chemical etching and design a process to obtain a specific etch rate and profile. (c)

14. Outline the parameters for dry etching of semiconductors and insulators and design a process that maximizes aspect ratio while minimizing damage. (c)
15. Calculate the effects of undercutting on minimum linewidth systems. (a)
16. Understand the implications of the binary phase diagrams of important elements and silicon and demonstrate the ability to calculate liquid and solid distributions by the lever rule. (c)
17. Relate the chemistry of phases to the solid solubility of impurities in silicon. (a)
18. Apply Fick's Laws to the thermal diffusion of impurities into silicon for both finite and infinite sources. (a)
19. Calculate the junction depth of diffused junctions in silicon including the effects of outdiffusion. (e)
20. Design the process time, species, and temperature for a desired pn junction diode cross section. (c)

By the time of Exam 5 (after 35 lectures) the students should be able to do the following:

21. Understand the process flow for the formation of a diffused bipolar transistor. (c)
22. Design the process times, species, and temperatures for a practical npn or pnp bipolar transistor. (c)
23. Explain the mechanisms for outdiffusion of impurities into a growing oxide layer. (a)
24. Evaluate the errors associated with critical steps in the thermal diffusion process. (e)
25. Design the diffusion parameters for a desired transistor working from the required diffused layer sheet resistances. (c)
26. Describe the mechanisms for impurity distribution under ion irradiation and calculate junction depths for typical implant conditions. (a)
27. Outline the advantages and disadvantages on various methods for removing the damage introduced by ion implantation. (e)

By the time of Exam 6 (after 43 lectures) the students should be able to do the following:

28. Explain the processes for chemical vapor deposition. (c)
29. Describe the mechanisms for, and importance of, selective oxidation and LOCOS. (c)
30. Calculate the rate of outdiffusion into a growing epitaxial layer and estimate the effect of outdiffusion on selected electronic devices. (a)
31. Design the process flow for isolation in modern IC devices (c)
32. Describe the methods and complexities for multi-level metalization and chemomechanical polishing (CMP). (c)
33. Define the critical issues that must be addressed in modern IC fabrication yield. (e)
34. Outline the salient features of statistical process control and show the relationship to modern IC fabrication. (a)

By the time of the Final Exam (after 43 lectures) the students should be able to do the following:

35. Fabricate a selection of IC devices including diodes, diffused capacitors, Schottky diodes, pn junction diodes, npn bipolar transistors, p-MOS transistors, n-MOS transistors, CMOS devices, and ring oscillators. (b), (d)
36. Understand and prove the limits of key process parameters including wet etch undercutting, minimum linewidth lithography, oxidation growth rates, and metalization coverage. (k)
37. Satisfactorily test and characterize the devices fabricated and apply statistical criteria to provide upper and lower limits to process sensitivity. (b), (d)