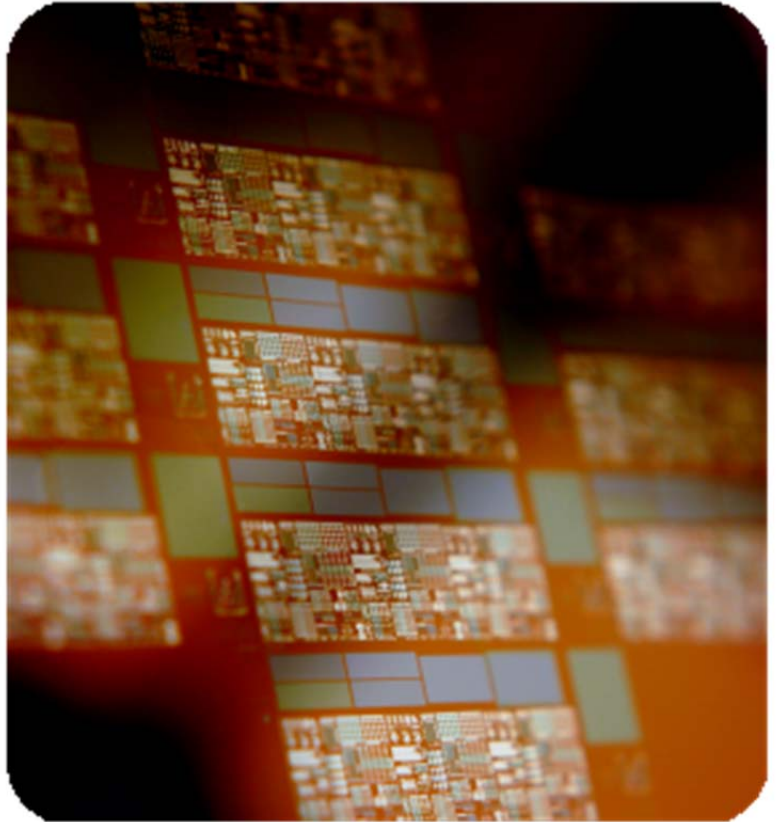
ECE444

Theory and Fabrication of Integrated Circuits Laboratory



Process Manual

Fall '24

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Testing Tutorial

This tutorial introduces the student to Keithley Clarius software and the probe stations. Later in the semester these skills will be used for electrical testing of student fabricated devices.

The goals of this tutorial is for the student to become familiar with

- Clarius electrical characterization software
- Test instruments
  - Keithley 4200-SCS Semiconductor parameter analyzer
- Probe stations
  - Microscope
  - Stage positioning
  - Micromanipulators

Three basic electronic devices will be tested:

- Commercial bipolar junction transistor (2N2222 npn BJT)
- Commercial n-channel metal oxide semiconductor field effect transistor (803 nMOSFET)
- Lab-fabricated Schottky diodes

The lab will be broken into three parts:

1. Testing commercial devices mounted in HP 16058A test fixtures
   - Practice using Clarius software with test instruments.
2. Using the probe stations to test Schottky diodes
   - Practice probing test pads using the microscope and micropositioners.
3. Performing transforms on the collected data.
   - Practice using advanced data analysis tools in Clarius.

Note: Depending upon the circumstances, it is possible that the tutorial will not be finished during the specified lab time. The transforms can be performed outside of class by remotely logging in using Remote Desktop – see http://fabweb.ece.illinois.edu/lab/testing/starting.aspx.

Testing Prelab Report

After reading through this Testing Tutorial (up to **COMMERCIAL DEVICE MEASUREMENTS***), the Appendices for the equipment (***APPENDIX A** *&* **J***), and the web links, answer the following questions.*

Evaporation Questions

Questions pertaining to equipment used for fabricating Schottky diodes: See Appendix B - LDS7211 Evaporator.

1. A turbomolecular pump is used to achieve ultra-high vacuum (UHV).
    a) What is the operational speed of the turbomolecular pump's rotor?
    b) How does this type of pump transfer gas from the inlet (chamber side) to the outlet (foreline side)?
    c) What is the ultimate pressure of the Leybold TMP1000C pump used in the LDS evaporator?
2. The pressure inside the chamber must be known in order to control the system properly.
    a) What types of pressure transducers are used on the LDS evaporator?
    b) How does each type work?
    c) Classify them according to pressure range.
3. Draw the piping schematic for a turbomolecular pumped vacuum system backed by an oil sealed rotary vane roughing pump. Include all necessary valves, pumps, and pressure transducers. Give the state (on/off) of the valves and pumps during standby, pumping down, and venting.

Electrical Test Questions

In the context of a test instrument, "compliance" tells the instrument 'how far to go' in order to comply with a measurement request. For example, if the instrument is programmed to sweep the voltage from 0 to 5 V, and the compliance value is set to 100 mA, the instrument will attempt to sweep the voltage to 5V, but will limit the current to 100 mA (the instrument then acts as a constant current source set to 100mA).

4. An instrument is programmed to measure the I-V characteristics of an ideal diode by sweeping the voltage from -5 to +5 volts in 10mV increments and measuring the current flowing through the device. The instrument's compliance is set to 5 mA.
    a) Create a plot of current vs. voltage that would result from the biasing conditions above using Microsoft Excel or other spreadsheet program. Use the ideal diode equation to calculate the current.

    $$I = I_0\left(e^{\frac{qV}{kT}} - 1\right)$$

    Assume that the reverse saturation current (I_0) = 1nA, the measurement is performed at room temperature, and that the current is not limited.
    b) Modify the plot by adding another data-set that reflects the output of the instrument, which is limited by the compliance set in the measurement conditions. Rescale the plot using values that place the compliance limited curve at approximately ½ of the full y-axis scale.

5. Refer to the manufacturer's web pages for data sheets for the following instruments used in the ece444 lab test stations:
   - Keithley 4200-SCS

   Specify the following items.

   a) Electrical parameters measured
   b) Maximum, minimum, and resolution of measured values

6. Remote Desktop into one of the lab workstations listed below. Instructions can be found in the Administrative Manual.
   – MNTL-260-K01.ad.uillinois.edu
   – MNTL-260-K02.ad.uillinois.edu
   – MNTL-260-K03.ad.uillinois.edu
   – MNTL-260-K04.ad.uillinois.edu
   – MNTL-260-K05.ad.uillinois.edu
   – MNTL-260-K06.ad.uillinois.edu

   Start Clarius as described in the **Initial Startup** section of this prelab (found below). Open the file **U:ECE444\Clarius_Files**. This needs to be copied to your U: drive from the V: drive via File Explorer.

   Using the Clarius model file and the device data sheets, find the following items:

   a) The range of collector voltages (start to stop) applied to the BJT in the BJT2N2222/Ic_vs_Vce setup.
   b) The highest voltage applied to all contacts in the Nmos model.
   c) Are these values within each device's ratings?

Clarius Commercial Device Measurements

Students perform simple I-V and C-V measurements on a 2N2222 general purpose BJT and a MTP2955 p-channel pMOSFET for this exercise. Information in this section is similar in nature to EXPLORING Clarius in **APPENDIX A**, but presented in a manner to step students through actual measurements.

Initial Startup

1. Log into the Keithley workstation using Active Directory credentials for the **UOFI** domain.
2. Open the PIV test fixture. One devices should be mounted in the lower test insert: either a BJT or Nmos. If both devices (or equivalent devices) are not present, contact the TA.
3. Inspect the sides of the PIV test fixture. Four triaxial SMU cables labeled SMU1, SMU2, SMU 3, and SMU4 should be connected to the corresponding jacks on the test fixture. If the SMU cables are not connected to the test fixture, contact TAs.
4. Check that the Keithley 4200A SPA is powered on. If not, press the power switch for the instrument. Before proceeding, wait for the instruments to finish power-on self-testing.
5. Start Clarius by clicking on START->KEITHLEY->CLARIUS if it does not start automatically.
6. Open the test file, which contains the test setup used for the Clarius Prelab and Final testing:
    a. In the **Clarius** main window, click on the Project button. The File window will open.
    b. Click left side to access directory. Navigate to **U:/Clarius_FILES.** Select the **444_tutorial_Final_Testing.krp,** then click **OPEN.**
    c. In the left list, select the device to be tested
7. Testing will begin with **Schottky Diode**, drop down the list to see tests to be performed.
8. Testing order in manual is under construction, please scan forward to find **Schottky Diode.**

BJT Measurements

The student will perform simple dc electrical characterization of a 2N2222A transistor mounted in the slots of the 16058A test fixture. The 2N2222A is a generic low-power npn BJT with a gain of ~150.

1. Open the cover of the test fixture and ensure the source monitor units (SMUs) connect electrically to the 2N2222. Close the cover to the test fixture.
2. In Clarius, open the BJT2N2222 tests by clicking the arrow by the label.
3. Measure and display I_c vs V_{ce} (family of curves):
    - Click **IC_VS_VCE**.
    - Select the **Configure** tab.
    - Check sweep ranges and compliances.
    - Select **Analyze** tab.
    - Click **Run**

    Clarius will configure the instruments and initiate a measurement. During this time the cursor will change to the 'busy' state. When the measurement is complete, the cursor will return to normal and the plot will be updated with measurement results.

When the measurement is complete, the displayed plot should look like a family of curves generated by a curve tracer.

The student should keep in mind that the devices are shared between lab sections, and as such may not be functional. If measured data is not what is expected based on theoretical understanding of the device, the TA should be notified.

If the student is not familiar with this type of measurement, they should contact the TA in charge of the Clarius Tutorial for an explanation of the curves.

4. *If the measured data is acceptable, the student should continue testing the BJT with the remaining setups listed in the* **SELECT DUT/SETUP** *window.*
   - *Vc-ib, Ve-ib*
   - *Early curves*
   - *Gummel curves*
   - *etc.*
5. *Upon completion of all measurements, the student should continue with nMOSFET testing below.*

n-channel MOSFET Measurements

The student will perform simple dc electrical characterization of a commercial SD210 nMOSFET.

1. Open the cover of the test fixture and ensure the nMOS is mounted in the lower test fixture and the source monitor units (SMUs) are connected. Close the cover to the test fixture.
2. In Clarius, Open the nmos setup in the lefthand list.
3. Measure and display I_d vs. V_g data:
   - Expand the **nMOS** DUT located on the left.
   - Click **ID_VG**.
   - Select the **Configure** tab.
   - Check sweep ranges and compliances.
   - Select the **ANALYZE** tab.
   - Select **RUN**

   When the measurement is complete, the displayed plot should appear similar to the family of curves generated for the BJT.

   Note that the spacing between the curves is not uniform. Why? If the student is unsure of the reason, they should reference a semiconductor physics text or ask for an explanation.

7. If the measured data is acceptable, the student should continue testing the nMOSFET *with the remaining setups listed in the lefthand window.*

Schottky Diode Measurements: An Introduction to the Probe Stations

The student will perform simple dc electrical characterization of a Schottky diode. The Schottky diodes to be tested are fabricated in the lab with the following parameters:

- Silicon wafer
  - 4" diameter wafer or pieces
  - N-type (phosphorus)
  - (100)
  - $\rho = \sim 1\ \Omega$-cm
- Rectifying contact (top)
  - ~2000Å aluminum
- Substrate contact (bottom)
  - N+ diffused layer (phosphorus)
  - ~0.3 µm diffused layer width
  - $R_s = \sim 10\ \Omega/\square$

The Schottky diodes are unpackaged, wafer-level devices which require the use of a probe station for testing. Each probe station contains four micro-manipulators and microprobes.

During testing, Probe 1 (connected to SMU1) will be used to make contact with the metal dot (anode) on the surface of the wafer, and the wafer chuck (connected to SMU2) will be used to make contact with the silicon substrate (cathode).
Note that SMU2 is normally connected to Probe 2. To connect SMU2 to the wafer chuck, a jumper coax cable must be used – on the probe stage, connect one end of the jumper to the jack labeled 'Chuck' and the other end of the jumper to the Cable labeled '2'.; Probe 2 should be raised so that it does not make contact with the wafer.

Loading the Schottky Diode

1. Turn on the LED ring light source located next to the probe station. Do not exceed 50% power.
2. Move the wafer chuck to the front of the probe station using the X-Y stage.
   - X positioning – rotate the knob farthest from the front of the probe station
   - Y positioning – rotate the knob closest to the front of the probe station
3. Place the wafer on the chuck using wafer tweezers.
4. Position the wafer using the X-Y stage so that it is roughly centered under the microscope.
5. While looking through the microscope, make adjustments to the wafer position to bring one of the metal dots into the microscope's field of view.

If the image through the microscope is dim or blurry, notify the TA for adjustment. Students should not attempt to make adjustments to the physical arrangement of the test stations, and will be penalized for making such adjustments.

6. Using the knob on top of the micropositioners, raise probes 2, 3, and 4 until the probe tips are located higher than the tip of probe 1.

7. Adjust probe 1 such that the tip *almost* touches the surface of the wafer. The student should observe the position of the probe tip at eye level (not through the microscope).

   This is a critical step and improper positioning can destroy the probe tips. The probes tips have a 5 µm tip radius and can be easily deformed if too much force is applied while in contact with a surface.

8. While observing through the microscope, use the knobs on the micromanipulator to place probe 1 into contact with the metal dot on the wafer surface. Adjustments are performed using the three knobs on the micropositioner:

   - X (in-and-out) – knob located on the back of the micropositioner; rotates around horizontal axis along the length of the prober body; clockwise rotation (to the right) moves tip closer to the micropositioner body; counter-clockwise rotation (to the left) moves tip away from micropositioner body.

   - Y (side-to-side) – knob located on the side of the prober body; rotates around horizontal axis along the width of the body; clockwise rotation (to the right) moves tip away from the front of the probe station; counter-clockwise rotation (to the left) moves tip toward the front of the probe station.

   - Z (up and down) – knob located on the top of the prober body; rotates around vertical axis; clockwise rotation (to the right) moves tip away from chuck; counter-clockwise rotation (to the left) moves tip closer to the chuck.

   The student will learn that using the probe stations is as much an art as it is a science, requiring dexterity and finesse. One of the trickier skills that students must develop is determining when the probe tip is actually in contact with the pads of a device.

   In ece444, one technique used to learn this skill is to drag the probe tip (away from the tip so that it does not 'dig in') to scratch the metal contact. It is obvious when the tip is not in contact.

   This technique is only for getting a 'feel' for probing, and should not be used once the student is more familiar with probing.

9. Once the probe tip is in contact with the metal, turn off the light source.

Measuring the Schottky Diode

Electrical characterization of the Schottky diode consists of three measurements performed in the following order:

1. Forward I-V using the SMUs to find a functional device. ->
2. C-V using CVIV module on the functional device. ->
3. Reverse I-V using the SMUs, which can potentially destroy the device.

Note that reverse I-V is the last measurement: there is the potential to destroy the device during this measurement due to the relatively high current density while in breakdown and the relatively high series resistance of the structure. Together, these issues can (and has) cause the metal contacts to be destroyed, preventing further testing. Thus, this test is performed after all other measurements are taken.

Forward I-V Measurement

1. In Clarius, Open the **SCHOTTKY** setup.
2. Within Clarius, run **IV configuration** file to connect the probes to the SMUs.
3. Measure and display $I_{forward}$ vs V data:
    - Click vfd.
    - Select the Configure tab.
    - Check sweep ranges and compliances.
    - Select the ANALYZE tab.
    - Select RUN

When the measurement is complete, the displayed plot should show a rectifying device (open circuit until the threshold voltage is reached, then acting as a short circuit).

Note that the Schottky diodes fabricated in lab are far from ideal:

- *High resistance due to low doping of substrate*
- *High contact resistance to backside*

These and other factors contribute to complex higher order effects at higher voltages, causing the curve to be distorted from what the student would expect. One of the main goals of this exercise will be to determine the turn-on voltage for the device, which is well below 1V. With this in mind, if the curve does not look as expected, reduce the sweep to an appropriate level.

C-V Measurement

After finding a working diode, the C-V characteristics of the device will be measured using the LCR meter.

1. Run **CV configuration** file to connect the probes to the CIV unit
2. Measure and display C vs V data:
    - Click **cv-diode**.
    - Select the **Configure** tab.
    - Check sweep ranges and compliances.
    - Select **Analyze** tab.
3. *Turn on the light.*
4. *Lower probes until the probe tips nearly make contact with the wafer – the student should observe this at eye level.*
5. *Final adjustments for contacting the probe to the device should be made with the use of the microscope and the micromanipulators.*
6. *Turn off the light.*
7. *Press* **Run** *in the Clarius software to continue the measurement.*

This calibration procedure needs to be performed only once during a testing session, unless there are changes to the arrangement of the LCR cabling (e.g. CMH is moved from probe 1 to probe 2).

When the measurement is complete, the displayed plot should show capacitance varying with reverse bias. The student should be able to predict the general shape of the curve using two basic equations:

$$C = \frac{\varepsilon A}{d}$$

$$w = \sqrt{\frac{2\epsilon(V_0 - V)}{q}\left(\frac{N_a - N_d}{N_a N_d}\right)}$$

Comments: A capacitor is a charge storing device consisting of two conducting plates of area A seperated by a dielectric of thickness d. In the case of a Schottky diode, the aluminum top contact acts as one plate and the substrate as another.

However, there is no physical dielectric added to the structure between the aluminum and substrate – i.e. the aluminum is in direct contact with the substrate. So why/how does the Schottky diode exhibit capacitance? The second equation should give you a hint (set d=w). If you are not familiar with it, consult a semiconductor physics book. Hint: this device can be used as a varactor…

3. If the measured data is acceptable, it is recommended that the student save the .mdl file as described previously. Continue to the next section.

Reverse I-V measurement

The last test to perform in the reverse breakdown I-V measurement. As mentioned previously, this is reserved as the final test as it may damage the device.

1. Measure and display $I_{reverse}$ vs V data:
    - Run iv_configure_Schotdiode
    - Click vrd
    - Select the **Configure** tab.
    - Ensure sweep ranges are correct.
    - Select **Analyze** tab.
    - Click **Run**.

When the measurement is complete, the displayed plot should show a rectifying device operating in the reverse bias region (open circuit until the device breaks down, then acting as a short circuit).

Note that the reverse breakdown voltage is dependent upon the substrate doping level. Higher doping reduces the breakdown voltage. This value can be useful when trouble-shooting issues with the C-V curves. Hint, hint..

Test Some More…

In order to account for variability in device characteristics across the wafer, repeat all three measurements on two other devices on the same substrate, saving the data as new models.

The student must physically move the wafer using the X-Y stage to probe additional devices.

1. In the **Clarius** window, select the **SCHOTTKY** icon.
2. Continue testing following the instructions above. Ideally three sets of good data.
3. When testing is complete for all three devices, continue to the next section.

Schottky Diode Calculations

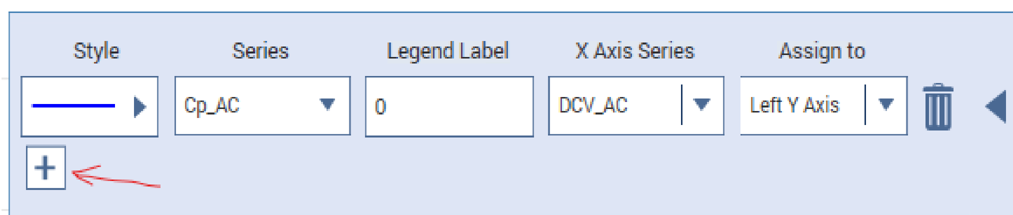
The measured electrical data acquired for the Schottky diodes is in of itself useful, giving graphical representations of the operating characteristics of the devices. However, much more information can be extracted from this data using relationships introduced in prior semiconductor physics courses/tutorials.

Clarius has a large library of built-in mathematical operators and functions that will be demonstrated and used to extract this information.

Note that this section of the tutorial requires Clarius to complete. However, students may not have time to complete this section while in the ece444 lab, requiring off-site Remote Desktop sessions. Instructions for remotely logging in can be found in the Administration Manual.

Calculation of V_0

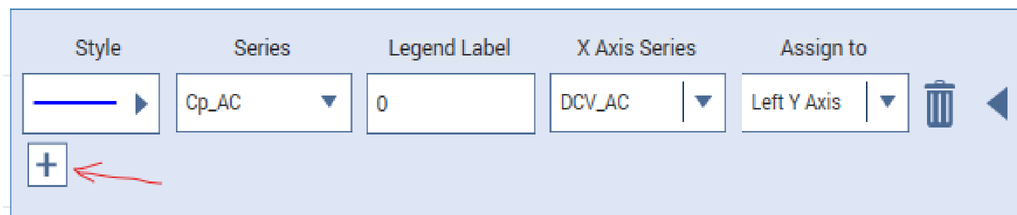
1. In the **Clarius** window, open the Schottky model by double clicking the **SCHOTTKY** icon.
2. Create a new plot in the **Cv_diode** setup:
   - Click on the **Analyze** Tab.
   - Click the **Formulator** button.
   - The **Formulator** window will open. Enter the following values (without quotes):
     - **Edit or Create New Formula** field: “logC=log10(Cp_AC)”
     - Click **Add/Update**
     - **Edit or Create New Formula** field: “logV=log10(0.1-DCV_AC)” - since V_0 is not known, a starting value of 0.1V will be used
     - Click **Add/Update**
     - Click **OK**
     - **Right click** on the graph to bring up menu, **Left click** on **Dual Graph**
     - **Right click** on the graph to bring up menu, **Left click** on **Data Series**
     - **Click** on the **+** sign to add a new function.



- Click **the arrow** to close the window . The new plot will be displayed in the main **Analysis** window.

3. Select the **logC_vs_logV** plot object.
4. Fit a line to the data in the new **logC_vs_logV** plot:
   - Place the mouse pointer over a point that is on the left side of the curve.
   - Right mouse click anywhere in the plot to display the menu.
     - Click on Line Fits
     - Select a linear fit, click ok, a dashed line with two points will appear on the plot. Several parameters will be displayed.
   - Note the slope of the line. This will be used in the next plot.
5. Create another new plot in the **C_vs_V** setup as described above, using the following values:
   - Edit or Create New Formula field "PowerLaw=cap^(1\[measured slope])"

     -Replace **[measured slope]** with the slope of the line fit from the **logC_vs_logV** plot.
   - Add this curve POWERLAW Series to the DCV_AC (x-data series) through the data series menu, and assign to the right Y axis



6. Fit a line to the data in the new **PowerLaw** plot as before. Note the x-intercept, as it will be used to revise the **logC_vs_logV** plot's **X Data**.
7. Revise the **X DATA** statement in the **logC_vs_logV** plot:
   - Using the absolute value of the x-intercept from the PowerLaw line fit, modify the plot definition as follows:
   - X DATA field: "log10([x-intercept value]-v_al)
   - The logC_vs_logV plot will be updated.

8. Iterate until solution is found:
    - Open the **logC_vs_logV** plot and fit a line to the new data. Note the slope.
    - Revise the **PowerLaw** plot definition:
        – **Y DATA** field: "cap^(1//**[new measured slope value]**)"
    - Open the PowerLaw plot and fit a line to the new data. Note the x-intercept and revise the logC_vs_logV plot definition again.
    - Repeat this process until both the slope and x-intercept do not change in value more than 5% between each iteration
9. Repeat the procedure for each device measured. The final values represent:
    - **X-intercept: solution for V_0 (should be ~0.3V)**
    - **Slope: grading of the junction (should be 0.35 – 0.5)**
10. Save all model files.

Calculation of Doping Concentration

The C-V plot can be used to calculate the doping concentration through the depletion region of the device. This requires the use of higher math functions which are available in the formulator.

1. In the **Clarius** window, open the Schottky model by double clicking the **SCHOTTKY** icon.
2. Create a new transform in the **C_VS_V** setup:
    - Click on the **DUTS-SETUPS** tab.
    - Expand the **CV** node In the **SELECT DUT/SETUP** panel, and then click on **C_VS_V**.
    - Click on the **EXTRACT/OPTIMIZE** tab.
    - Click the **NEW…** button.
    - The **PROMPT DIALOG** window will open: enter a name in the **TRANSFORM NAME** field. For this example, "Deriv_Trans" will be used.
    - Click **OK**. The **PROMPT DIALOG** window will close, and the new transform will be listed by name in the **SELECT TRANSFORM** pane.
    - Select the new transform by clicking on its' name in the **SELECT TRANSFORM** pane.

- Enter “derivative” In the **FUNCTION** field, then press <ENTER>.
- Three entry fields will be appear in the pane directly below the **FUNCTION** field. Enter the following values (without quotes):
  – **X DATA** field: “v_al”
  – **Y DATA** field: “(cap//**[area of diode]**)^-2” – replace [area of diode] with the calculated area of the diode in cm^2 (the diameter of the diode is ~0.025”).
  – **ORDER** field: “1” - for first order derivative
- Click on the **EXECUTE** button to perform the calculation. This creates a dataset that can be used for further calculations or plotting.

3. Create another new plot in the **C_vs_V** setup as described above, using the following values:
   - **PLOT** field: “DopingProfile”
   - **X DATA** field: “11.9*8.85e-14***[area of diode]***cap^-1”
     – Replace **[area of diode]** with the actual area of the diode calculated above.
   - **Y DATA** field: “-2//(11.9*8.85e-14*1.6e-19)***Deriv_trans**^-1”
     – Replace **Deriv_Trans** with the actual name given to the transform.
4. Open the new plot:
   - The curve displayed is the concentration of the substrate as a function of position within the substrate – a ‘doping profile’.
   - The distance over which the concentration is calculated is limited by the width of the depletion region.
   - The concentration values (y-axis) should be close to $10^{15}cm^{-3}$. If not, entered values should be checked and the area of the diode recalculated, ensuring that the units of area are cm^2.
5. Repeat the procedure for each measured device.
   - Hint: transforms and plot setups can be saved as files and imported.
6. Save all model files.

ECE444 Process Recipe

Introduction

The student will produce a variety of electronic devices and circuits in this experiment. A special mask set was designed for the fabrication of more structures than he or she could possibly test and analyze during the semester. Each mask contains 45 complete copies of the appropriate layer of the device cell. Three cells are combined into what is known as a field. A test area has been included in each field to monitor and map intermediate processing parameters. You should look at Appendix I to see which parts of the test area to use for measurements at different stages of the process.

The class will be split into three groups which will start at different stages of the fabrication and testing. On the fifth meeting of the semester, everyone could be at the same step and requiring the same piece of equipment. Fortunately, people work at different paces and will probably be staggered enough to minimize such "collisions". *It will be in your best interest to come prepared to proceed as far as possible in the process each period*.

-Cleanliness is of utmost importance in the fabrication process. Contaminants introduced during the process can degrade or destroy device performance. Therefore, it is important that processing equipment or chemicals are never touched with the bare hands, (i.e., diffusion furnaces, push rods, boats, etc.). Not only do the bare hands contain dirt and oils, but also sodium, which can easily destroy FETs (*why?*). Always handle the wafer with clean tweezers. A good rule to remember is to never touch anything with your bare hands that will come in contact with the wafer.

-Always consult the instructor if any mistakes are made in processing. Always consult your instructor at the beginning of the period for any special processing instructions. Often the instructor will call a short meeting at the beginning to make such announcements to everyone at once.

-Photoresist should not be left on wafers overnight. Do not begin a photoresist operation unless you are confident you can finish it. At the beginning of the semester a PR patterning process will take a little over an hour. Later, it will go quicker.

Processing Overview

In addition to reading the description below, you can also look at schematic cross-sections of a FET and BJT at various stages in the ECE444 process. The cross-sections should be useful in understanding the purpose for the various processing steps.

The first step will be to clean and oxidize a batch of wafers in a group of three students. The wafers will be referred to as the "IC wafers" in this recipe. A pattern will be etched through the oxide using Mask 1 and the Photoresist (PR) process outlined in the manual. The wafer will then be subjected to a boron ambient at high temperature so that the boron will diffuse into the N-type silicon through the ‘holes’ in the oxide, forming P-regions on the wafer in those areas delineated by Mask 1. This diffusion is known as the predeposition or *predep* diffusion.

After the wafer has been suitably cleaned and excess boron removed, it will be subjected to another diffusion, called the redistribution or *drive* diffusion, this time without the boron source. The idea here is to move the dopant farther into the wafer. This diffusion will be made in an oxygen atmosphere so that *another layer of oxide is grown simultaneously* on the wafer to mask the P-regions from subsequent doping processes.

After suitable cleaning, a second PR process using Mask 2 will be used to delineate areas which will be changed back to N-type by a phosphorus predeposition diffusion. The third mask will be used to remove oxide from the gate regions of the FETs so that a thin high quality gate oxide may be grown there.

Mask 4 will be used to etch holes down to the various regions through which metal contacts to the silicon surface can be effected. Mask 5 will be used to define the aluminum contact areas, and then aluminum will be vacuum evaporated over the entire wafer. The photoresist will be removed, *lifting off* the metal in the unwanted areas. Scale drawings of these masks are available for study in Appendix I of this manual. The ECE444 homepage on the World Wide Web (*http://fabweb.ece.uiuc.edu*) contains an interactive image of the mask set, which can be very useful in exploring the various regions of the mask set.

Finally, you will form ohmic Al-Si contacts by annealing. This is a process in which the components of a system are heated to a temperature *below* the system's eutectic point. (The melting point of a given alloy of one substance in another depends upon the percentages of the materials present. That point on a phase diagram of temperature vs. percent of each parent material present where a temperature minimum occurs in the liquidus line is known as the eutectic point. The eutectic point for the Al-Si system is 576°C.) You will use a temperature of 475°C, which permits the aluminum atoms to move around and spread more uniformly over the silicon surface. In addition, during annealing, the aluminum can diffuse into the silicon itself. Annealing is used instead of alloying (i.e., heating of the system to temperatures *above* the eutectic point) because experience in our lab has shown that alloying often has a detrimental effect on the resulting p-n junction diode characteristics (find out about *Al spiking* on your own).

The devices will then be tested, and operational chips noted for further testing.

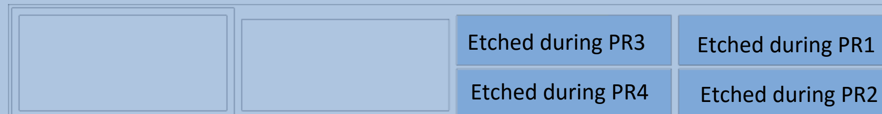
Cleanroom etiquette

- Minimize the number of materials brought into the cleanroom.
    - At most, a lab manual, notebook, and a pen may be brought into the lab.
- Students should wait in the pre-gowning area if there are three people already in the gowning room. This is due to space limitations in the gowning room.
- Safety glasses must be worn in the lab at all times. Prescription glasses are suitable alternatives.
- Wearing of contact lenses is not allowed while working in the lab. Students with contact lenses must wear prescription glasses or personally owned sealed safety goggles.
- While gowning, try to prevent cleanroom garments from touching the floor. Cleanroom boots should not touch the 'dirty' side of the bench. Students may use the gowning bench to 'swivel' from the 'dirty' to the 'clean' side of the bench while donning these boots.
- As you enter the cleanroom, take a couple of steps on the tacky mat to remove lint from the booties.
- Entry to the wet lab requires 'thin' gloves and a face shield. 'Thick' gloves must also be worn if working in the fume hoods in the wet lab.

Oxidation Pre-Lab Report

Turn in the answers to the following questions before carrying out the procedures in the rest of this section.

1. What are the purposes of the SC-1 and SC-2 solutions in the RCA standard cleaning procedure? Refer to the article by Kern in Appendix C.
2. As an alternative to the RCA clean, a clean which uses a sulfuric acid-hydrogen peroxide solution followed by an HF step has been proposed. List 5 advantages of this substitution. (See Pieter Burggraaf's article "Keeping the 'RCA' in Wet Chemistry Cleaning" in the appendix C of the paper version).
3. Refer to the oxidation step below. What gases are flowing during
   a. dry oxidation?
   b. steam oxidation?
4. In steam oxidation, how is the steam produced?
5. Oxidation thicknesses:
   a. Determine the field oxide thickness of the wafer after each oxidation step in the complete recipe. Use the oxidation charts. Tabulate the results in an Excel spreadsheet.
   b. Determine the oxide thickness for each of the four test windows (shown highlighted below) after the wafer is finished processing. Use the oxidation charts. Tabulate the results in an Excel spreadsheet. **You will need to reference the mask set (available on the web site and in the Last page of Operations Procedures Manual (pg143))** for each mask level to see what areas have been etched away before each oxidation step.



   c. Add another column to the spreadsheet and add the color of the oxide in that area. Use GT-7 as a reference.

   The surface plane of your silicon wafer is (100), so use the (100) curves.

   Note: *If a dry oxidation step is off the chart you may assume its contribution is negligible. Such assumptions should always be clearly stated, however!*

Oxidation may not have been covered in lecture yet, so here is some help: The graphs show thickness as a function of time, given as ($t+\tau$). If there is already oxide present on your wafer before a certain oxidation step, "τ" is the equivalent time required under the current oxidation conditions (temperature, steam or dry...) to give that oxide thickness. The oxidation step is of duration "t". To find the thickness after the oxidation step, you need to use $t+\tau$, and read the corresponding thickness off the appropriate curve.

Oxidation example: Suppose that you are to do a 12 minute steam oxidation at 1100° C, and there is already 0.19 μm oxide present. From the (100) curve on GT.6, 0.19 μm corresponds to T = 8 min. (In other words, it is as if you have already done 8 minutes in steam at 1100° C to give you the 0.19 microns already present.) Then add t = 12 min to T = 8 min to get t+T=20 min. At t+T = 20 min, read the 1100° C curve to get a final thickness of 0.34 μm. (Note that the value of T would be different for a different temperature, or for dry oxidation.)

6. Explain in general terms why different thicknesses of oxide give different colors. Why is it important to view samples vertically? (see Anner section 5.10 and GT-7)

Starting Material Information

The following is the wafer spec sheet submitted to SQI for our wafers. Be sure to record the parameters for the starting material (substrate and epitaxial layer).

*An epitaxial layer is a thin layer of single crystal Si grown on the much thicker single crystal Si substrate. The doping of the "epi-layer" is generally different in type and/or concentration from that of the substrate. –**Note: the wafers used in lab do not have an epi layer.***

Supplier: **Silicon Quest, International**

1230 Memorex Drive

Santa Clara, CA 95050

408.496.1000

http://www.siliconquest.com

Manufacturer: various

	substrate	units
resistivity	1-5	Ω-cm
doping material	Phosphorus	
thickness	500-550	μm
orientation	(100)	

Determine the background doping of the substrate using the ρ vs. N graph in the GT section (GT-1). Enter the background doping for the substrate in your online-logsheet at the first opportunity.

N_C = ____________ cm^{-3} (from GT-1 and starting material information)

What are the advantages of using (100) orientated wafers? When would (111) orientation be preferred?

What are epitaxial layers used for?

Degrease Tweezers and Wafers

The Clean Air Act reduced the production of trichloroethane (TCA), which is a major constituent of the degreasing procedure. There are alternatives, namely trichloroethylene (TCE) and methylene chloride, both of which are or possibly are carcinogenic. Your lab instructor will update you on the method of degreasing.

Your instructor will have a Teflon® holder loaded with an appropriate number of wafers. The degreasing procedure is posted on the degreaser hood and can be found in appendix C.

Remove Native Oxide

The instructor will have some extra words of caution just before your first experience with the strong acids in the ECE 444 lab. Heed them and be careful!

1. Perform a 30-second oxide etch in the 50DI: 1HF acid under the acid Etch Hood to remove any oxide which may have been built up due to exposure to air.
2. DI rinse in the HF Rinse tub under the Acid Etch Hood.
3. Spray rinse. Be sure to spray off any HF that may have gotten on the handle.

What is native oxide? Why must it be removed?

RCA Cleaning

Clean the wafers using the RCA standard clean in Appendix C.

The procedures are posted on the wet lab's acid hoods, so please do not take your lab manual, notebook, or PDA into the wet lab. All you have to remember are the general steps, which in this case are to degrease, remove native oxide, and RCA clean.

Why is it important to remove ionic impurities? What devices does this type of contamination affect? What affect will they have on the performance of the devices?

Oxidation

The oxidation consists of a dry oxidation step, a steam oxidation step, and a final dry oxidation step. The dry oxide is higher quality, but the steam oxide grows more quickly. You will be doing the oxidation as a group. The lab instructor will demonstrate the loading and unloading procedure first.

1. After a careful review of the instructions regarding the furnaces given in appendix G of the paper version, a student should insert the wafers into the steam oxidation furnace (T=1100°C) with nitrogen flowing.
3. One group member should be assigned to time keeping and switching gases. Once the wafers have reached the center of the furnace:
   - Turn ***on*** the O_2 and turn ***off*** the N_2 (the lower gas panel in the gas cabinet). With only O_2 flowing, the wafers will undergo *dry oxidation*. Let the wafers soak for 15 min with only O_2 flowing.
   - Turn on the H_2 so that both O_2 and H_2 are flowing. This combination will produce steam from the combustion of the gases (pyrogenic steam), and the wafers will undergo *steam oxidation*. Let the wafers soak with steam for 30 min.
   - Turn off the H_2 to revert back to a dry oxidation. Let the wafers soak for 10 min with only O_2 flowing.
   - Switch back to N_2 only (turn ***on*** the N_2, then turn ***off*** the O_2).
4. A different student should remove the wafer boat.
5. Each student should remove one wafer and hold it in the air for 10 - 20 seconds before placing it into their wafer carrier. (The cool down time is essential to avoid melting of the wafer carrier!)
6. The timekeeper should place the boat back into the furnace. Everyone should get some experience handling the quartzware. Further practice is also encouraged. Later on, you'll be doing things on your own without the 1:3 teacher student ratio - take advantage of the instructor now.

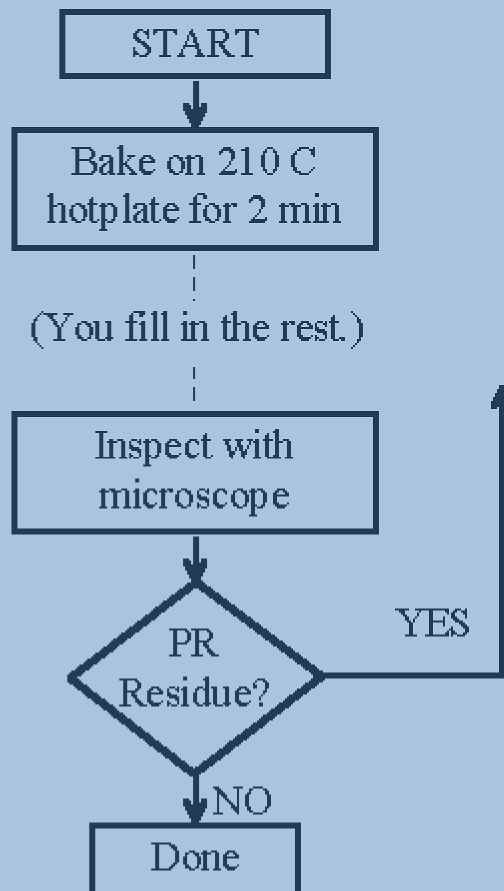
What is the purpose of starting and stopping with a dry oxidation?

What are the mechanical and electrical differences between dry and wet thermally grown oxide?

Photoresist 1 Prelab Report

These questions are to be turned in before beginning the first photoresist patterning of the IC wafer.

1. Draw a flow chart of the basic positive PR process used for opening windows in unpatterned oxide for ECE 444. *This includes etching the oxide and removing the PR*. Use concise descriptions or names for each *significant* step. Refer to Appendices D and H. You will be using Acetone for PR removal. For those who do not know what is meant by a flow chart, an example is shown. Just enough detail should be included to allow you or some other ECE 444 graduate to reproduce the process a year from now without the benefit of the lab manual excerpts we post in the lab. For the amount of detail we are looking for, your flowchart should fit on one page. **It should also contain three conditional loops. (For example, see the one below for PR residue.)**



2. The test instruments in the lab are limited to ±200V. Calculate the electric field across the final field oxide (the oxide which is never etched away) at this voltage. Does this field exceed the breakdown field of the oxide? Assume that the oxide will breakdown in an electric field of 10^7 V/cm (a conservative figure). Show your work.

3. Outline the alignment procedure used by the UltraTech 1000WF stepper as described in Appendix H. Categorize the steps as either mechanical or optical.

Degrease the IC Wafer and Tweezers

Cleanliness is extremely important. Tweezers and wafers should always be degreased at the beginning of a processing session. Appendix C of the paper version describes the degreasing procedure and is posted in the wet lab. Do not take paper into the wetlab, please.

PR 1 - Open Windows for First Diffusion

1. Follow the procedure for putting a patterned layer of photoresist on the wafer given in Appendix D.
2. Etch the oxide using $6NH_4F$:1HF (BOE) for 5.5 min. Slowly agitate the wafer carrier back and forth during the etch. Do NOT splash! Rinse in DI water thoroughly, and N_2 dry.

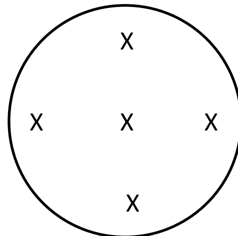
   Wet etching requires the diffusion of the etchant to the surface and the diffusion of the reaction products away from the surface. The smallest windows on the wafer will etch at a rate closer to that of the large test areas with a little rotational agitation.

   When coming out of the etch it is important to let the wafer carrier drip for a few seconds while no more than a few centimeters above the acid. Tilting the carrier in two opposing directions also helps return more acid to its container. This not only keeps the DI rinses cleaner, but also minimizes the depletion of the acid container.

Is wet etching of SiO_2 isotropic or anisotropic? What consequences will this have on linewidths? How will this affect the different devices?

4. Use the hot point probe (see Appendix E) in the upper right window of the test areas to check for complete oxide removal.

   If time permits, check in 5 areas such as this:



This will ensure uniformity in etching by mapping over the entire wafer.

If no definitive reading (a few nanoamps or more) is obtained, etch in 30 second intervals until oxide is removed. Do not etch for more than 6 minutes without consulting your instructor.

What sign should the ammeter reading be?

5. Always follow up with a microscope inspection to insure that all the windows to be opened through the oxide are indeed etched to bare silicon. The test area should be uniform in color (metallic grey) and all the opened windows should match it.
6. Record the wafer type (p or n) determined using the hot point probe.

   Type = ________.

7. Initial PR Removal: Hold your wafer level over the waste acetone/IPA container (with the lid off) and squirt acetone on the wafer until it begins to flow off the edges. Let it dissolve the PR for 10-15 seconds before draining the acetone into the waste container. Repeat until most of the PR is gone (~3 times).
8. Strip off any remaining PR residue by following the standard degreasing procedure (Acetone, IPA, DI, IPA, N_2 dry.) Make sure you remove residue where your tweezers were.
9. Inspect the wafer under a microscope for PR residue. Go back and degrease if necessary. Incomplete photoresist removal is the most common cause of furnace tube contamination. *Please inspect wafers thoroughly.*

Boron Predeposition

1. Degrease the wafer.
2. Perform a 10-15 second etch in 50:1 DI:HF if it has been more than an hour since opening the diffusion windows, DI rinse, and N_2 dry.
3. Check the boron predep furnace and support equipment (i.e., gas flows and temperature). The boron predep furnace should be at 950°C.
4. Follow the procedure for furnace loading in appendix G of the paper version. Use the Boron predep furnace and load the wafer so that the patterned side is facing the nearest BN wafer. Be sure to record which position your wafer is in (see Appendix G.4). *Don't forget the stainless steel endcaps!*
5. After a 15 min predeposition at 950°C, unload your wafer.
8. Use the LDS four-point probe to determine the sheet resistance. Use the '*Single Measurement*' measurement type. Input the correct system parameters into the appropriate fields: the width of the window is 2.4mm, probe spacing is 40mils, use DifCAD to calculate diffusion depth. Consult the instructor if the measured value is outside the range 70-120 ohms/square; you may have to return the wafer to the furnace.

   Note: The correction factor was determined for the smaller of the four point probe windows (second large window from left – see illustration that follows).

   Note: this measurement does not always give a valid value at this step. Borosilicate glass (BSG) forms during predeposition and does not conduct. Normally the BSG breaks down during this measurement, but it may be of sufficient thickness to prevent breakdown. If this happens, you may use the Veeco 4PP with 'auto-penetrate' selected. The Veeco applies a 170V spike before measuring to ensure breakdown of any insulating films.

   R_s=__________ ohms/square.

How is boron deposited on the wafer during the predep? What is the boron solid source composed of?

Note: The BN source transfers boron to the wafer via B2O3. The B2O3 reacts with the silicon to form a heavily doped SiO2 layer (borosilicate glass), with a B:Si alloy layer at the BSG – Si interface. The BSG is easily removed with BOE, but the B:Si layer must be oxidized chemically before it can be removed with the BOE.

This transfer of boron using B2O3 is the ideal case for the ECE444 lab, but can be greatly accelerated by the presence of H2 or H2O. The hydrogen reacts with B2O3 to form HBO2 (meta-boric acid), which has a vapor pressure much higher than B2O3. The higher vapor pressure of the metaboric acid accelerates the growth rate of BSG, therefore requiring a longer BSG etch.

Remove Borosilicate Glass

1. Clean the wafer for the drive diffusion and testing using the following procedure. (The idea here is to remove the borosilicate glass and any elemental boron formed on the wafer surface during predep.) The original thermally grown oxide is not removed, but it is etched slightly. Check with your TA to see if there are additional instructions.
   - Remove the borosilicate glass by placing the wafer in the 50:1 DI:HF oxide etch for 15 seconds. Follow with a thorough DI rinse.
   - Immerse the wafer in 1 H_2SO_4 : 1 HNO_3 for 10 minutes to oxidize the Si:B layer.
   - **Rinse thoroughly with DI water** and return to the 50 DI:1 HF oxide etch for 30 seconds to remove the oxidized boron. If HNO_3 is transferred to the HF, it becomes a silicon etch.
   - Wash very thoroughly in DI water and dry carefully with N_2.
2. Perform a hot-point probe measurement on any open region in the test area of the wafer. You may want to map the wafer again for a more thorough test. Record whether it is P or N type. (Refer to Appendix E in the paper version.)
   Also, make sheet resistance measurements on the wafer with the LDS four point probe using '*Pattern Measurement*' as the measurement type, '*Simple*' as the test pattern, and the previous system parameters. Record the sheet resistance values to the logsheet database as 'Boron Predep Rs' using the supplied utility. Consult Appendix F in the paper version if necessary.

   Boron predep. Type ____________ R_{s1} = ____________ ohms/sq.

   When filling out the logsheet an SPC chart appears beside the form. This chart will give you an idea of whether your sheet resistance values are consistent with historical data. There are three horizontal lines: the average (X-bar) and 3σ (sigma) above and below X-bar. Your value should fall within ±3 σ of X-bar. If the measured value is out of this range consult your instructor. Your wafer may be returned to the boron predep furnace for an additional 10 minutes depending on the how far it deviates from the average.

   Did the Borosilicate glass affect the four-point probe measurement?

What is borosilicate glass?

Boron Drive

1. Have your instructor check the boron drive furnace and support equipment (i.e., gas flows). The furnace should be at 1100°C.
3. Degrease your wafer using the instructions in Appendix C of the paper version.
4. Insert wafer into boron drive furnace using Appendix G of the paper version as a guide.
5. Perform the following drive recipe at T = 1100°C. (20 minutes total drive time).
   - Dry oxygen drive for 10 min.
   - Steam drive for 30 min.
   - Back to a dry drive for 5 min.

There are multiple processes occurring during the boron drive. What are they?

PR2 - Open Windows for Phosphorus Predeposition

Dark field masks are mostly dark when held up to a light. Since we want the holes in the chrome layer on the mask to be transferred as holes in the PR, a positive photoresist is needed. SHIPLEY 1813 PR is inherently a positive resist so processing is relatively simple and robust. The drawback of a dark field is that, since its mostly dark, you can't see much of the underlying wafer with which you are to align - for contact aligning, this is important when using contact aligners. However, since we are using the steppers, this is of no consequence to the process.

Light field masks, being mostly clear, are easily aligned with the underlying wafer using a contact aligner, but for masks 1 through 4 a negative PR would need to be used.

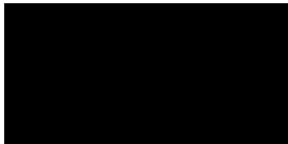
1. Use the photoresist process to transfer the pattern from mask 2 into the oxide. Note that this time there is a pattern to which to align, and Run Mode 2 is used. Expose the PR to a **150mW-sec/cm^2** dose of ultraviolet energy (this has been determined empirically to obtain the best resolution). Use an oxide etch time of 6 min before checking with the hot point probe for etch completeness. (Be sure to use the proper etch solution for the oxide.) Don't forget to complete the pattern transfer by removing the PR (as stated in Appendix D of the paper version).

   The hot point probe measurement should always be done in a region of the test area which originally had the thickest oxide to be etched. There are two oxide thicknesses present on the wafer at this point. For subsequent mask layers there will be a larger number of various thicknesses.

The hot point probe measurement alone is NOT *a sufficient condition to stop etching. The wafer should always be inspected under a microscope (preferably without filtered light.) Check many places on the wafer to verify that all the windows which are supposed to be open are uniform in appearance and identical in color to the hot point probe test area for that layer. Of course, the inspection requires familiarity with the mask set. Study the mask set so you know what to expect.*

3. Measure the sheet resistance of the boron diffusion with the LDS four point probe using the leftmost window just opened for the phosphorus diffusion using '*Pattern Measurement*' as the measurement type, '*Simple*' as the test pattern, window width = 2..9mm, 40mil probe spacing, and calculate the junction depth using DifCAD. Record the sheet resistance values to the logsheet database as 'Boron Drive Rs' using the supplied utility.

   Your measured sheet resistance value will be approximately 2x to 4x the previous measured value. Why?



Wafers with PR on them should NOT be probed with the four point probe. Poor aim can render the tips insulating and thereby yield false results to several students.

R_s = __________ ohms/square.

Phosphorus Predeposition Diffusion

1. Degrease one more time and inspect carefully for complete PR removal. Contamination of the furnace can affect more than just your wafer. In addition to the wafers of innocent students, there is several thousands of dollars worth of quartzware and source wafers which could be ruined.
2. If it has been more than an hour since opening the diffusion windows, perform a 10-15 second etch in 50:1 DI:HF, DI rinse, and N_2 dry.
3. Perform a phosphorus predeposition diffusion at 1000°C for 25 min. The gases are switched for you. Nitrogen flows at the standby rate for the first 15 min, then switches to oxygen for the remaining time (it leaves the nitrogen on the entire time). A low oxygen concentration (~5%) is used in order to minimize the phosphorus silicide formation described in 7.12 of Anner. The contribution to the field oxide thickness may be ignored for prediction purposes. Record the actual flow rates in your electronic logsheet.

4. Use the LDS four-point probe to determine the sheet resistance. Use the '*Single Measurement*' measurement type. Input the correct system parameters into the appropriate fields: the width of the window is 5.5mm, probe spacing is 40mils, use DifCAD to calculate diffusion depth. Consult the instructor if the measured value is outside the range 10-40 ohms/square; you may have to return the wafer to the furnace.

   R_s= _________ ohms/square.

   Which area should you measure?

Remove Phosphosilicate Glass

1. Phosphosilicate glass is supposed to be considerably easier to remove than borosilicate glass, but we'll use the same procedure to remove it. High surface concentrations of phosphorus are detrimental to photoresist adhesion so it is imperative that we remove it all.
   - Remove the phosphosilicate glass by placing the wafer in the 50:1 DI:HF oxide etch for 20 seconds. Follow with a thorough DI rinse.
   - Immerse the wafer in 1 H_2SO_4 : 1 HNO_3 for 10 minutes.
   - Rinse thoroughly with DI water and return to the 50 DI:1 HF oxide etch for another 10 seconds.
   - Wash very thoroughly in DI water and dry carefully with N_2.
2. Measure the sheet resistance of the phosphorus diffusion with the LDS four point probe using the leftmost window just opened for the phosphorus diffusion using '*Pattern Measurement*' as the measurement type, '*Simple*' as the test pattern, window width = 2..9mm, 40mil probe spacing, and calculate the junction depth using DifCAD. Record the sheet resistance values to the logsheet database as 'Phosphorus Predep Rs' using the supplied utility.

   R_s= ________ ohms/square.

3. Use the hot point probe to verify that the largest test area (on left) has indeed been changed back to N-type. Consult your instructor if it did not.

PR3 - Open Windows for Gate Oxidation

Use the photoresist process to transfer the pattern from mask 3 into the oxide. Use the 3-minute bakeout option to help recover the loss of PR adhesion due to the high phosphorus concentrations. Increasing the hard-bake time to 2 minutes may also aid the PR adhesion. Use an oxide etch time of 6 min before checking with the hot point probe for etch completeness. As in PR-2, expose the PR to a 150mW-sec/cm^2 dose of ultraviolet energy.

There tends to be excessive undercutting during the oxide etch due to poor adhesion of the PR to areas containing phosphorus. What consequences will this have on the devices?

Gate Oxidation

1. Degrease your wafer before this critical step. If we were going to employ one more RCA clean in this process, this is where it would be. If time permits, we will perform another RCA clean at this point. Ask your instructor.
2. Grow 250 Å of dry oxide at 1000°C in the newly opened windows. Use the gate oxidation furnace. It's up to you to calculate the oxidation time. Use the <100> curve to figure out the necessary oxidation time and check with the instructor to see if this is correct (it is also a good idea to manually calculate the time using Grove’s model in GT-8 and/or use the Grove calculator on the web). Check that the O_2 flow is correct (110±10). If it is not, notify your instructor. During the oxidation, take the opportunity to familiarize yourself with the workstations and/or fill in your logsheet file.

Oxide Thickness Measurements

Since all the high temperature steps are completed, anytime you are waiting for other equipment you should use the ellipsometer and thin film measurement system to measure all the various oxide thicknesses on your wafer. The test areas should be sufficient for this purpose except when you have unpatterned aluminum on the wafer. Consider this a "filler" activity that MUST be completed in time for the final report.

PR4 - Open Contact Windows

1. Use the standard photoresist process to transfer the pattern from mask 4 into the oxide. Use an oxide etch time of 6.5 min before checking with the hot point probe for etch completeness. As in PR-1, expose the PR to a 150mW-sec/cm^2 dose of ultraviolet energy. Don't forget to follow- up with a thorough microscope inspection. An incomplete etch here may result in device failure, particularly in the schottky diodes so check them carefully. A short 15-30 second overetch after a positive inspection will help ensure good contacts.
3. Use the LDS four-point probe to determine the sheet resistance. Use the '*Single Measurement*' measurement type. Input the correct system parameters into the appropriate fields: the widths of the windows are: phosphorus - 2..5mm, boron – 2.4mm; probe spacing is 40mils; use DifCAD to calculate diffusion depth. Record to 'Final Phosphorus Rs' and 'Final Boron Rs' respectively.
   - R_{sboron}= _________ Ω/□
   - $R_{Sphosphorus}$= _________Ω/□

What β do you expect from your BJTs given the measured sheet resistances? How does this compare with the β predicted from DIFCAD?

A Time for Contemplation

You are nearly finished! Congratulations. But… do you know what you have really done up to this point? Now is a good time to think about all of the processing steps.

Try this: draw a cross-sectional diagram of the wafer for both a BJT and a FET. Draw and label what occurs for each step (including oxide layer thicknesses, silicon consumption, junction depths, etc.). Don't forget to include the consumption of silicon during oxide growth!

Processing Report

The purpose of this report is to show that you know what has been going on inside the wafer during processing. In addition, the questions have been designed to help you see how the various processing steps are related to device parameters. This is a very important part of process design. If something is not clear to you, ask! Completing this report should be educational, not merely a contest!

1. Use Difcad to *help* construct a band diagram of your vertical BJTs at equilibrium. Show the collector and emitter contacts (and everything in between) and depletion regions in the diagram. *You may neglect showing the base contact because it cannot be elegantly presented in the same band diagram.* Calculate the energy levels at several points in each region of the structure.

   Note that DIFCAD will only give you the net doping profile. You must use that information to calculate the energy bands. This can easily be done by using an Excel spreadsheet, but be careful about depletion regions! They are not so easily included, and must be calculated and drawn in.

2. List all the processing reasons (other than contamination) you can think of that may cause the real energy bands in your fabricated device to be different from what you determined above. Understanding the limitations of the theories you use is almost as important as the theories themselves. For each of the processing steps, think about what actually goes on, but is not included in your DIFCAD calculations. (For example, why is the base doping profile not the same as what is calculated in DIFCAD?)

3. Draw the cross section of one of your P-channel FETs. *Include all significant regions while the device is biased in saturation*. Your diagram should show at least the following items:
   - lateral diffusion of dopants
   - diffusion depths
   - the channel
   - depletion regions
   - varying oxide thicknesses, labeled with thicknesses
   - height variations of the silicon surface, due to consumption during oxidation
   - some idea of lateral dimensions

   The horizontal and vertical scales should not be the same. Why? You may use the (100) oxidation curves or oxide thicknesses measured using the ellipsometer. Be sure to state whether you are using the measured or calculated thicknesses.
4. Draw a detailed cross section of one of your BJTs unbiased and at equilibrium. Be sure to state whether you are using the measured or calculated oxide thicknesses. Your diagram should show at least the following:
   - lateral diffusion of dopants
   - diffusion depths
   - depletion regions
   - varying oxide thicknesses, labeled with thickness
   - height variations of the silicon surface, due to consumption during oxidation

- some idea of lateral dimensions

5. The ECE 444 recipe compromises the performance between the three main transistor types. In this question, you will explore the effects of processing parameter changes on the performance of the different transistor types present on your wafer:
   - Construct a table like the one below. Fill in the table by listing the effect that each processing step has on the physical device parameters (after all processing is completed) if the time or temperature is increased.

     Note: x_{jC} and x_{jE} are the junction depths of the collector/base and emitter/base junctions, respectively, W_b is the base width, and C_i is the capacitance of the insulator in the gate of the FETs.

     Note that some steps will not affect some parameters.

	x_{jC}	x_{jE}	W_b	$\|N_d-N_a\|$ in n-type regions	$\|N_d-N_a\|$ in p-type regions	C_i
Initial Oxidation						
Boron Predep						
Boron Drive						
Phosphorus Predep						
Gate Oxidation						

-

Construct a second table like the following one. Fill in this table by listing the effect that each physical device parameter has on the electrical performance characteristics of the device (like Beta, V_t...) if the time or temperature is increased. (Note: an N-channel MOSFET has an n-type source and drain.)

	β of BJTs	$\|V_t\|$ of p-channel MOSFETs	$\|V_t\|$ of n-channel MOSFETs	R_{series} of p-channel MOSFET source and drain
x_{jC}				
x_{jE}				
W_b				
$\|N_d-N_a\|$ in n-type regions				
$\|N_d-N_a\|$ in p-type regions				
C_i				

6. Use your tables from above to aid in determining specific changes to the recipe you would make in order to improve the performance of each type of transistor (e.g. increase time of _____ in order to....) (These should be changes to the processing parameters only, not to the mask layout.) Do not specify processes which you cannot perform in the ECE 444 facility (e.g. ion implantation). Specifically:
   - What change(s) would you make to improve the performance of the npn BJTs, and how will that affect the performance of the P-MOSFETs and N-MOSFETs.
   - What change(s) would you make to improve the performance of the P-MOSFETs, and how will that affect the performance of the N-MOSFETs and npn BJTs.
   - What change(s) would you make to improve the performance of the N-MOSFETs, and how will that affect the performance of the P-MOSFETs and npn BJTs.
7. The ECE 444 device layouts compromise the performance of the three main transistor types for the sake of processing tolerance. For each type of transistor (NPN BJTs, N-MOSFETs, and P-MOSFETs) describe or illustrate a single change to the layout you would make in order to improve its performance in some way. Briefly discuss the ramifications of your proposed changes if they were implemented (e.g. less misalignment tolerance). Look closely at the device cell mask set in Appendix I.
   - BJTs: (Hint: The distance between contacts is relatively large. What does that do to device performance? How could you change the layout to improve the performance? What effect does that have on processing tolerance?)
   - P-MOSFETs: (Hint: The gate oxide and metal overlap the Source and Drain regions. What does that do to device performance? How could you change the layout to improve the performance. What effect does that have on processing tolerance?)
   - N-MOSFETs

Define Metal Contacts

The method for metal definition used in class is called lift-off. The photoresist is applied and exposed using a darkfield mask to define areas where the aluminum will contact the silicon and form contacts. Aluminum is then evaporated over the entire wafer, and the PR is then removed. The aluminum will stick to the silicon, but will "lift off" where it has deposited on the photoresist. There are problems with this method, mainly unwanted step coverage (i.e. the aluminum forms a continuous layer over the entire wafer) due to sloping photoresist walls. This will cause unwanted removal of the aluminum in contact areas. To overcome this problem, undercutting of the photoresist is desired, and can be achieved by several methods.

1. If more than an hour has passed since PR-4, remove the native oxide with a 10-15 second dip in the 50:1 DI:HF, DI rinse, and N_2 dry.
2. Spin photoresist onto the wafer as usual in preparation for exposure. As in PR-1, expose the PR to an 150mW-sec/cm^2 dose of ultraviolet energy through Mask 5.
3. <OPTIONAL>Before developing, perform a 3 minute soak in chlorobenzene (check with your instructor to see if this step will be performed).

What is the chlorobenzene for? It forms a 'skin' on the top surface of the photoresist which is less soluble in developer. Therefore, it develops more slowly than the PR beneath, causing undercutting, which in turn reduces the possibility of step coverage and the undesirable lift-off of the contacts.

Warning: chlorobenzene should not be inhaled. Perform this under the solvent hood only.

4. Develop as normal.
5. Don't forget to follow-up with a thorough microscope inspection. *Do not perform the hardbake - it will only increase the amount of time required to remove the PR and lift off the metal.*

Aluminum Evaporation for Contacts

1. In the LDS 1820 evaporation system, load the wafer into the holder directly above the aluminum (pattern side <u>down</u>), manually pump down and evaporate all the Aluminum as per Appendix B in the paper version. Approximately 2000 Å should be deposited.
2. Vent and remove wafer for inspection.

Lift-off Aluminum

1. Place the wafer into the container marked *Lift-off Acetone*.
2. Make sure the wafer is covered entirely with acetone and soak for 10 minutes. The aluminum will begin to 'peel off.' Slight agitation of the container will help lift-off the metal. If the aluminum has not completely lifted off after 10 minutes, take a swab and gently wipe the wafer to remove the metal.
3. Degrease your wafer after all excess aluminum has lifted off.

Anneal Contacts

1. Adjust N_2 flow to 100 on the flowmeter if it is not there already.
2. Load your wafer into the annealing furnace for 15 minutes at T =475°C.
3. When the 15 minutes have elapsed, remove the wafer from the furnace and place it in your wafer carrier. Be sure that the boat pushrod is fully inserted into the quartz tube so that it will not be broken. Return the empty boat to the front of the furnace tube.

Electrical Testing

Electrical testing will be accomplished in two waves. Since there are only 5 test stations, only 5 in each section will make measurements on the basic device types at a time. When everyone is done with the set of fundamental semiconductor measurements, the remainder of the semester will be spent on more advanced measurements.

Review appendix J in the paper version for tips on the proper operation of the probers. Refer to the website or the ICS Tutorial for help in using ICS.

There is also information there about

- which BJTs to test
- which FETs to test,
- which Capacitors to test,
- which Diodes to test,

as well as which probes to place on the contacts. It is suggested that you start with the devices that are most likely to work (FETs and capacitors).

Understand and fill in each data set with data from 3 of each device type (although the number may be modified depending on time constraints – ask your instructor). The three types of FETs it takes to fill in one model are sufficient for the first round of testing.

One part of the measurement setups not covered well in the ECE 340 text are the gummel plots for the BJTs.

Gummel plots are simply the display of the natural log of base and collector currents as V_{be} and $V_{ce}(=V_{be})$ are varied simultaneously . The collector and base potentials are kept identical and the currents measured independently as the emitter potential is swept. The base current will display the characteristic regions of thermal recombination-generation dominance at low currents ($I=I_o\, e^{(qV/2kT)}$), quasi-ideal ($I=I_o\, e^{(qV/kT)}$), and current limiting ohmic effects at high currents. The corresponding collector current through these ranges can tell a lot about how useful the BJT will be for certain applications. The ratio of the two currents, beta, will usually have a peak somewhere in the middle, the broader the better. It can tell the circuit designer how sensitive the device is to the bias point.

The additional advanced testing will be handled using a handout when it seems clear just how much time will be available.

Final Report

The questions here are intended to help you learn about the devices you fabricated and tested. Of course, they are also used as a means for assessing what you have learned. If something is not clear to you, ask! Completing this report should be educational, not merely a contest!

NOTE: In this report, as in any engineering level report, state your assumptions clearly. Making reasonable assumptions is OK, but you must clearly state and justify them. Full credit cannot be given in cases where, say, the voltage reference direction is important, but not stated. Pictures often help in clearing up such ambiguities. Device location information is also important if verification of results is to be possible. Show all work in the written report.

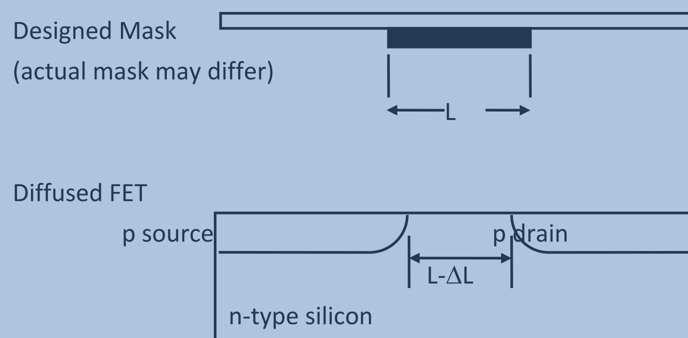
This report will be submitted partially in electronic form. No printouts of the ICS files or your logsheet file will be necessary except for your own benefit. In the questions that ask you to generate plots in ICS, be sure to save the plots in your file. After completing the items below, you are to submit your data files to your via email.

Even if your wafer didn't work or work completely, do the best you can with answering the questions and completing the tasks below. We can't give partial credit for answers like "my BJTs didn't work".

1. LOGSHEET: Enter or verify all the process variables in the logsheet on the web. In your lab notebook, enter any observations and conclusions you can make from the data. Do not make up numbers if you missed collecting some of them. The data will be used to demonstrate Statistical Process Control concepts.

2. After fabrication of your FETs, the actual gate lengths are shorter than the designed gate lengths as drawn using the CAD system. The diagram below shows the designed gate mask and the gate region of one of your diffused p-channel FETs. The designed gate width drawn on the CAD system is L, and L-ΔL is the final (actual) gate length.

   Note: the designed mask is not necessarily the same as the actual mask.



a) Think about all of the steps that come between designing a mask using a CAD system and the final (diffused) device. Why is the actual gate length shorter than the length in the CAD drawing for the mask? (i.e., what causes ΔL?) There are several contributing factors.

b) What happens if ΔL is greater than L? How does that show up while testing the device?

c) What was the shortest gate length device that worked on your wafer? What upper bound does that place on ΔL? What is a reasonable lower bound?

d) For two FETs in the same device cell, nearly the same amount (ΔL) is subtracted from the gate length for each device. In other words, ΔL does not depend on L. It is possible to determine the discrepancy between the actual and the as designed channel lengths from measurements of two different FETs. Create plots (in ICS) of gm (transconductance) vs. vg in the *large* and *short* FET setups. Use a transform to do the derivative (i.e., to calculate gm). The slopes of the gm curves in the saturation region are functions of the channel lengths. (Be careful about what the saturation region is!) The relationships may be found in Streetman's text. Find ΔL.

3. Ideality factor of diodes:

a) Create a plot called **ideality** in the Ifwd_vs_V test of the diodes setup to plot the ideality factor, *n*, from equation 5-71 in section 5.6.2 of Streetman:

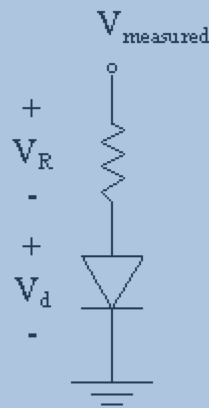
$$I = I_o\left(e^{qV/nkT} - 1\right)$$

where *V* is the voltage across the junction, I_o is the reverse leakage current, and *n* is the ideality factor.

b) Plot *n* vs. current. Use GT.19 for the value of kT/q. I_o may be taken as the leakage current with a reverse bias of 1 volt (the value can be found on the data spreadsheet of the test). Use the transform editor to create a plottable dataset for n and enter it into the Y-data of a plot.

c) Why shouldn't you plot the ideality factor vs. voltage? (There is a practical reason related to the way testing is done. Try it if it is not immediately obvious).

d) The voltage you measured for your diode includes the series resistance of the contacts and the n and p-type material on each side of the junction in addition to the voltage across the junction itself. The voltage used in equation 5-71 of Streetman should be only the voltage across the junction, whereas the entire measured voltage was used in the plot you created. Make a correction to the equation to take the series resistance into account. The forward series resistance of your diode can be determined from the slope of the I-V curve in the linear, high-current region. For each diode, use the value of the resistance to make a new plot called **ideality _corrected**, which plots the ideality factor vs. current, eliminating the voltage due to series resistance.



e) What effect does correcting for the resistance have on your ideality plots?
f) What is the effect of using a smaller value for Io in your ideality plots?
g) What do expect to see in the ideality plots (see Streetman)? Do you see it?

4. For a one-sided step junction, the junction capacitance is given by

$$C = A\left[\frac{q\varepsilon_s}{2(Vo - V)}N\right]^{1/2},$$

where A is the area, V is the applied voltage (V < 0 for reverse bias), and N is the doping on the lighter-doped side.

For a one-sided junction with linear grading on the lighter-doped side, the junction capacitance is given by

$$C = A\left[\frac{q\varepsilon_s^{\,2}}{3(Vo - V)}G\right]^{1/3}$$

where G is the grade constant (slope of N at the junction). (See Streetman.) Real diffused junctions are somewhere between these two cases.

a) What should the slope of a log(C) vs. log(V_o-V) curve be for a one-sided step junction?
b) What should the slope of a log(C) vs. log(V_o-V) curve be for a one-sided junction with linear grading?
c) For each C-V plot of the pn junctions (in the diodes setup), plot log10(C) vs. log10(V_o-V) using ICS, where V is referenced as a positive voltage under forward bias. Refer to the band diagram in your Processing Report to make an initial guess for V_o. Improve your estimate for the built-in voltage for each pn junction by extrapolating a plot of $C^{(1/slope)}$ vs. V to the x-axis, where "slope" is the slope in the high voltage region of your first plot. Use ICS to generate and fit the plot. Plug the new value for V_o back into the first plot and iterate this process until you get the same value out of the second plot (within a few percent). Note: if you cannot reasonably fit a line to the entire voltage range, use the high voltage regions.
d) Compare the slopes of your log(C) vs. log(V_o-V) curves for the emitter/base and collector/base junctions. What does this say about your junctions? Is it what you would expect?

5. Include all appropriate graphs in the submitted report. You can take screenshots or replot the data using a program such as Excel or Origin.

6. Capacitor breakdown: Determine the breakdown *field* of the capacitors from your measured breakdown voltage and the oxide thickness for each of the three methods of determining oxide thickness. Use the oxide thickness as determined in the following three different ways. Discuss any discrepancies between them. Use the oxide thickness:
   a) predicted by the appropriate oxidation curves,
   b) determined by the ellipsometer measurement,
   c) determined by the thin film measurement system, and
   d) calculated from your measured capacitance vs. voltage curves.
7. There is a great deal of information contained within your measured capacitance vs. voltage curves. In this question, you will extract some of the information, including the doping level of the silicon substrate. See Streetman or any other reference concerning MOS capacitors. (Note that in this question, the capacitances are **NOT** per unit area, as they are in Streetman.) You can find information about the capacitor area by using the interactive mask set on the ECE444 website.
   a) What is your measured value of the insulator capacitance, C_i?
   b) What is your measured value of the total capacitance, C_{min}, when the capacitor is biased such that the depletion region is at maximum width?
   c) What is happening in the portion of the C vs. V curve where C is not constant? (i.e., what is changing in the device that causes the capacitance to vary?)
   d) From your values of C_i and C_{min}, what is the value of the depletion capacitance, C_d, when the capacitor is biased such that the depletion region is at maximum width?
   e) From C_d, what is the maximum depletion width, wm, of the capacitor?
   f) At what measured value of voltage does the capacitor reach maximum depletion width, and what parameter of an FET should that voltage correspond to?
   g) From the maximum depletion width, wm, find the doping concentration, N_d, of the silicon substrate.
   h) How would your measured C vs. V curve be different if:
      - The substrate was p-type?
      - the doping level was higher?
      - the gate oxide was thicker?
8. How do the threshold voltages from the FET measurements compare with those from the capacitor B measurements? Which would you trust more?
9. Compared to the single diffused diodes you measured (C-B junction), what differences would you expect if you:
   (1) used a substrate contact several device cells away?
   (2) measured the round Schottky diode?
10. List all the effects you can think of which cause the geometry of the various regions of the final devices to differ from the CAD layout. (Note that not all of these reasons will be processing mistakes.)
11. DIODES: Compare the values of the built-in voltage obtained in the following three ways:
    a) V_o determined from your capacitance data (log[C] vs. log [V_o-V] curves.)
    b) V_o determined by extrapolating a line from the linear portion of the forward I-V characteristics of the junctions.
    c) V_o predicted by the BJT band diagram in your processing report.
    d) Compare and discuss ALL the possible reasons you can think of for discrepancies between the background doping levels determined from the manufacturer's stated value of the starting epi-layer resistivity and the capacitor measurements.

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